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(71)出願人　000001122
国際電気株式会社
東京都中野区東中野三丁目14番20号

(71)出願人　390010515
株式会社鷹山
東京都世田谷区北沢３－５－18　鷹山ビル

(72)発明者　占部　健三
東京都中野区東中野三丁目14番20号国際電気株式会社内

(72)発明者　周　長明
東京都世田谷区北沢３－５－18　鷹山ビル
株式会社鷹山内

(74)代理人　弁理士　山本　誠

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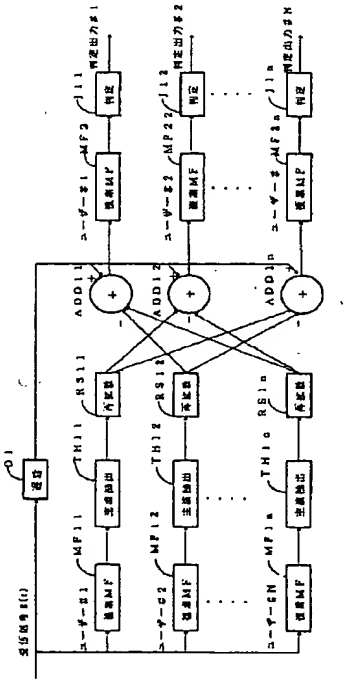
(54)【発明の名称】　マルチユーザー復調方法および装置

(57)【要約】

【目的】　干渉キャンセラを用いることなく同期に関する問題を解消し得るマルチユーザ復調方法および装置を提供する。

【構成】　受信信号を逆拡散した信号を閾値処理して特定ユーザの信号を抽出し、この抽出された信号を再拡散し、特定ユーザ以外の再拡散信号を受信信号から減ずる。その結果特定ユーザの信号を抽出する。



【特許請求の範囲】

【請求項１】　Ｎ個（Ｎは自然数）の移動局のためのＤＳ－ＣＤＭＡ方式による多重通信を行う際に、各移動局に対応したＮ個の第１、第２マッチドフィルタを基地局の受信機に設けておき、各第１、第２マッチドフィルタには対応する移動局に割り当てられた拡散符号をタップ係数として設定し、受信信号を第１マッチドフィルタで処理し、その出力を閾値処理して所定レベル以上の出力を抽出し、この抽出された出力を当該拡散符号により再拡散し、前記受信信号と再拡散された信号が同期するように受信信号を遅延させ、この遅延された受信信号から（Ｎ－１）個の再拡散出力を減じて、他の１個の移動局の拡散符号を有する第２マッチドフィルタに入力し、各第２マッチドフィルタの出力から各移動局の信号を判定するマルチユーザ復調方法。

【請求項２】　マルチユーザ数がＮ局（Ｎは自然数）であるＤＳ－ＣＤＭＡ方式を多重方式とする基地局の受信機に設備される装置であって、

それぞれのユーザに割り当てられたスペクトラム拡散のための拡散符号をタップ係数とし、受信信号を入力しながら相関取得演算を行うＮ個のユーザー抽出用の複素マッチドフィルタと、

該Ｎ個のユーザー抽出用複素マッチドフィルタから得られる各々のユーザーの相関結果から電力の大きい到来波成分（以下、主波という）を抽出するＮ個の主波抽出回路と、

該Ｎ個の主波抽出回路から得られる主波成分を用いて再度当該拡散符号によりスペクトラム拡散を行う再拡散回路と、

受信信号を所定の処理時間だけ遅延させる遅延回路と、

上記Ｎ個の再拡散回路の出力のうち当該ユーザー以外の出力を全て上記遅延回路の出力から差し引く各々Ｎ個の加算器と、

それぞれのユーザーに割り当てられたスペクトラム拡散の為の拡散符号をタップ係数とし、該Ｎ個の加算器の出力を入力しながら再度相関演算を行うＮ個のユーザー復調用複素マッチドフィルタと、

該Ｎ個のユーザー復調用複素マッチドフィルタの出力からユーザー毎の信号を判定するＮ個の判定回路と、

を備えたことを特徴とするマルチユーザー復調装置。

【請求項３】　閾値処理は、第１マッチドフィルタの相関出力信号の最大電力に対する所定比率により設定されていることを特徴とする請求項１記載のマルチユーザー復調方法。

【請求項４】　主波抽出回路はユーザー抽出用複素マッチドフィルタの相関出力信号の最大電力に対する所定比率の閾値による閾値処理を行うようになっていることを特徴とする請求項２記載のマルチユーザー復調装置。

【請求項５】　複素マッチドフィルタ回路はＩ成分、Ｑ成分それぞれのための２個のマッチドフィルタよりなり、各マッチドフィルタは：

（ａ）入力電圧に接続されたスイッチと、このスイッチの出力に接続された第１キャパシタンスと、この第１キャパシタンスの出力に接続された奇数段のＭＯＳインバータよりなる第１反転増幅部と、この第１反転増幅部の出力を入力に接続する第１帰還キャパシタンスと、前記第１反転増幅部の出力または基準電圧を択一的に出力する第１マルチプレクサと、この第１マルチプレクサの出力とは逆の選択で第１反転増幅器出力または基準電圧を出力する第２マルチプレクサとを有する複数のサンプル・ホールド回路と；

（ｂ）各サンプル・ホールド回路の第１マルチプレクサの出力が接続された複数の第２キャパシタンスと、これら第２キャパシタンスの出力が統合されつつ接続された奇数段のＭＯＳインバータよりなる第２反転増幅部と、この第２反転増幅部の出力を入力に接続する第２帰還キャパシタンスとを有する第１加算部と；

（ｃ）各サンプル・ホールド回路の第２マルチプレクサの出力および第１加算部の出力が接続された複数の第３キャパシタンスと、これら第３キャパシタンスの出力が統合されつつ接続された奇数段のＭＯＳインバータよりなる第３反転増幅部と、

この第３反転増幅部の出力を入力に接続する第３帰還キャパシタンスとを有する第２加算部と；

（ｄ）前記第１加算部の出力から第２加算部の出力を減ずる減算部と；

（ｅ）前記サンプル・ホールド回路のうちいずれか１個における前記スイッチを閉成するとともに他のスイッチを開放しかつ所定の組合せで各サンプル・ホールド回路の第１、第２マルチプレクサを切り換えるコントロール回路と；を備えていることを特徴とする請求項１または２記載マルチユーザ復調方法または装置。

【請求項６】　マッチドフィルタ回路は、受信信号が入力された複数の遅延回路と、各遅延回路の出力に接続され当該出力にＰＮ符号を乗ずる乗算回路と、これら乗算回路の出力を加算する加算回路とを備えていることを特徴とする請求項１または２記載のマルチユーザ復調方法または装置。

【請求項７】　乗算回路は、受信信号に並列に接続された複数のインピーダンスと、各インピーダンスの出力に接続されたスイッチと、これらスイッチが反転入力に並列に接続されかつ非反転入力が接地された演算増幅器と、この演算増幅器の出力を前記反転入力に帰還させる帰還インピーダンスとを備え、前記スイッチはＰＮ符号に応じて選択的に閉成されることを特徴とする請求項６記載のマルチユーザ復調方法または装置。

【請求項８】　演算増幅器の出力には１入力２出力の符号用スイッチが接続されこの符号スイッチの第１の出力には符号用入力インピーダンスが接続され、この入力インピーダンスの出力には符号用演算増幅器がその反転

入力において接続され、この符号用演算増幅器の出力は符号用帰還インピーダンスを介して前記反転入力に接続され、符号用帰還インピーダンスは符号用入力インピーダンスと等しく設定され、ＰＮ符号が正のときには符号用スイッチは第１の出力に接続されて符号用演算増幅器の出力が乗算結果とされ、ＰＮ符号が負のときには符号用スイッチの第２の出力が乗算結果とされることを特徴とする請求項７記載のマルチユーザ復調方法または装置。

【請求項９】　加算回路は、各乗算回路の出力が接続された加算用入力インピーダンスと、これら加算用入力インピーダンスの出力が反転入力に並列に接続されかつ非反転入力が接地された加算用演算増幅器と、この加算用演算増幅器の出力を前記反転入力に接続する加算用帰還インピーダンスと、を備え、加算用帰還インピーダンスは加算用入力インピーダンスと等しく設定されていることを特徴とする請求項６記載のマルチユーザ復調方法または装置。

【請求項１０】　遅延回路は複数のサンプル・ホールド回路を初段から最終段まで直列に接続し、受信信号をこの初段から入力して順次最終段まで転送するようになっている請求項２または６記載のマルチユーザ復調装置。

【請求項１１】　サンプル・ホールド回路は、バッファ回路、サンプル・ホールド用スイッチを交互に直列に接続し、各スイッチの出力に接地キャパシタンスを接続してあることを特徴とする請求項１０記載のマルチユーザ復調装置。

【請求項１２】　バッファは非反転入力が入力とされ、出力が反転入力に帰還された演算増幅器よりなることを特徴とする請求項１１記載のマルチユーザ復調装置。

【請求項１３】　バッファは入力用インピーダンスと、この入力用インピーダンスの出力が反転入力に接続されかつ非反転入力が接地された演算増幅器と、前記入力用インピーダンスと等しく設定されかつこの演算増幅器の出力を前記反転入力に帰還させる帰還用インピーダンスとよりなることを特徴とする請求項１１記載のマルチユーザ復調装置。

【請求項１４】　主波抽出回路は非反転入力に受信信号が入力され、反転入力に閾値電圧が入力された演算増幅器であることを特徴とする請求項２記載のマルチユーザ復調装置。

【請求項１５】　主波抽出回路は受信信号と基準電圧とを択一的に出力するマルチプレクサと、閾値電圧の反転と受信信号とを加算する容量結合とを備え、前記マルチプレクサはこの加算結果に応じて切換え制御されることを特徴とする請求項２記載のマルチユーザ復調装置。

【請求項１６】　再拡散回路は、入力電圧が接続されたスイッチと、このスイッチの出力を反転する第１反転バッファと、この第１反転バッファの出力を反転する第２反転バッファと、第１反転バッファまたは第２反転バッファのいずれか一方の出力を択一的に出力するマルチプレクサとを備えている請求項１または２記載のマルチユーザ復調方法または装置。

【請求項１７】　再拡散回路は、入力電圧が接続されたサンプル・ホールド回路と、このサンプル・ホールド回路の出力が１入力２出力のスイッチと、このスイッチの第１の出力に接続された反転バッファとを備えている請求項１または２記載のマルチユーザ復調方法または装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＤＳ－ＣＤＭＡ（Ｄｉｒｅｃｔ　Ｓｅｑｕｅｎｃｅ－Ｃｏｄｅ　Ｄｉｖｉｓｉｏｎ　Ｍｕｌｔｉｐｌｅ　Ａｃｃｅｓｓ）方式のスペクトラム拡散通信における基地局の受信機のためのマルチユーザー復調装置に関する。

【０００２】

【従来の技術】ＤＳ－ＣＤＭＡ方式スペクトラム拡散通信の基地局受信機では複数ユーザーからの信号を受信し、干渉等を考慮しつつ各ユーザーの信号を分離抽出し、抽出された信号を逆拡散する必要があるが、従来比較的単純な回路よりなるスライディングコリレータ（Ｓｌｉｄｉｎｇ　Ｃｏｒｒｅｌａｔｏｒ：以下ＳＣという）を用いて逆拡散のための相関演算を行うことが多かった。そしてＳＣは入力信号の拡散符号と受信機の拡散符号との位相同期が完璧であることが要求され、ＤＬＬ（ＤｅｌａｙＬｏｃｋｅｄ　Ｌｏｏｐ）等の同期捕捉・保持回路が必要であった。しかしＤＬＬは初期引き込み時間および再引き込み時間が大であるという欠点を有し、また一般に完璧な同期を実現することは困難であるので、同期の不完全さによる受信特性の劣化が生じた。

【０００３】さらに各ユーザーの信号間の干渉を防止するために、従来、干渉キャンセラが使用されていたが、この干渉キャンセラは受信信号の逆拡散、レイク合成等の処理を経た後に、スペクトラム拡散によって個々のユーザの信号に対応した受信信号を再現し、特定ユーザー以外のユーザーの再現信号を受信信号から減ずることにより特定ユーザーのための受信信号を抽出するものであったが、回路が極めて大規模かつ高価であった。

【０００４】

【発明が解決しようとする課題】本発明はこのような従来の問題点を解消すべく創案されたもので、同期に関連した問題点を解消し、かつ干渉キャンセラが不要なマルチユーザ復調方法および装置を提供することを目的とする。

【０００５】

【課題を解決するための手段】本発明に係るマルチユーザ復調方法は、受信信号を逆拡散した信号を単に閾値処

理することによって特定ユーザーの信号を抽出し、抽出された信号を再拡散し、特定ユーザー以外の再拡散信号を受信信号から減ずることにより特定ユーザーのための受信信号を抽出するものである。

【０００６】

【発明の実施の形態】次に本発明に係るマルチユーザ復調方法の１実施例を図面に基づいて説明する。

【０００７】

【実施例】図１は本発明に係るマルチユーザ復調方法の１実施例を概念的に示すものであり、複素マッチドフィルタＭＦ１１、ＭＦ１２、．．．、ＭＦ１ｎにおいて受信信号Ｒ（ｔ）を逆拡散して各ユーザーの信号を抽出する。ここで抽出された各ユーザーの信号は伝送路による歪みを受けており、さらに受信信号には熱雑音が含まれている。ここに伝送路歪みを考慮した各ユーザーの信号をＩｉ（ｔ）、その受信レベルをａｉ、各ユーザーの拡散符号をＰＮｉ、熱雑音をｎ（ｔ）とすると、受信信号Ｒ（ｔ）は、

【数１】

$$R(t) = a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \ldots + an \cdot PNn \cdot In(t) + n(t) \qquad (1)$$

と表現される。

【０００８】例えば第１のマッチドフィルタＭＦ１１によって受信信号Ｒ（ｔ）を処理すると、図２の実線の出力電圧が生じ、この出力電圧には１周期（１シンボル時間）ごとに複数のピークＰ１、Ｐ２、Ｐ３が現われている。実線で示される電圧は式（１）の第１項および熱雑音項と第１ユーザ拡散符号との相関演算結果である。また一点鎖線は干渉波電圧であり、式（１）の第２項～第ｎ項の和と第１ユーザ拡散符号との相関演算結果である。

【０００９】一般にＤＳ－ＣＤＭＡ方式では各ユーザーに与えられる拡散符号は直交性が高く、相互相関が低いため干渉波のレベルは低いが、ユーザー数が増加すると干渉波のレベルは図２に示すように高くなり、正確なピーク検出が困難となる。

【００１０】そこでマッチドフィルタＭＦ１１～ＭＦ１ｎの出力は主波抽出部ＴＨ１１、ＴＨ１２、．．．、ＴＨ１ｎに入力され、干渉波および熱雑音を強制的に除去する。ここに主波抽出は閾値処理であり、概念的には、図２におけるピークＰ１～Ｐ３のうちＰ３を、所定レベル以下のピークとして消去して、図３のような波形を生じさせる処理である。但し、実際の閾値処理では閾値以下の入力は低レベルの信号に変換されるので、実際には図３８あるいは図４０の出力が生じる。主波抽出部は１シンボル時間内の最大電力を与えるピーク電圧に対して所定の比率を掛けた電圧を閾値として受信信号を閾値処理する。主波抽出部の出力は再拡散部ＲＳ１１、ＲＳ１２、．．．、ＲＳ１ｎにそれぞれ入力され、再度スペクトル拡散が行われる。この再拡散出力は個々のユーザーのための受信信号に近似したレプリカ信号であり、例えばＲＳ１１の出力は第１番目以外のユーザーのためのレプリカ信号である。

【００１１】以上のレプリカ信号を用いて、各ユーザーのための拡散信号を生成する。すなわち、第ｉ番目のユーザーのための拡散信号の生成においては、第ｉ番目以外のユーザーのレプリカ信号の和を、加算器ＡＤＤ１ｉにおいて、受信信号Ｒ（ｔ）から減算する。受信信号Ｒ（ｔ）は遅延回路Ｄ１により遅延され、マッチドフィルタ、主波抽出部、再拡散回路による処理結果とのタイミングが調整されている。仮にレプリカ信号が理想的な状態、すなわち式（１）の第ｉ番目の項のみが抽出されたとすると、加算器出力は式（２）に示すように、第ｉ番目のユーザーのための拡散信号成分と熱雑音の和となる。

【数２】

$$\begin{aligned} Aouti &= R(t) - \{a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \ldots + ai-1 \cdot PNi-1 \cdot Ii-1(t)\} \\ &\quad - \{ai+1 \cdot PNi+1 \cdot Ii+1(t) + \ldots + an \cdot PNn \cdot In(t)\} \\ &= ai \cdot PNi \cdot Ii(t) + n(t) \end{aligned} \qquad (2)$$

式（２）から明らかなように、加算器の出力において、相互相関、すなわち干渉の影響を軽減し得ることが分る。

【００１２】このように抽出された拡散信号成分は複素マッチドフィルタＭＦ２１、ＭＦ２２、．．．、ＭＦ２ｎによって相関演算され、理想的には、受信信号における各ユーザーの逆拡散信号成分が抽出される。この相関演算結果に対して判定回路Ｊ１１、Ｊ１２、．．．、Ｊ１ｎにおいて、対応ユーザーの信号の存在を判定し、その信号を出力する。

【００１３】ここで、マルチパスが生じていない場合の種々のマッチドフィルタ出力を通じて図１の実施例の効果を示す。

【００１４】図４は干渉が極めて少ない場合の前記マッチドフィルタＭＦ２１の出力のシミュレーション例を示す。ここにシミュレーションの条件は、１次変調ＱＰＳＫ、拡散符号１２８チップＭ系列、オーバーサンプル数４、ユーザー数２局とし、ベースバンド帯での静的条件の下での相関演算である。同図において、ｔ＝０のときに第１番目のユーザー（希望局とする。）の相関ピークが検出されている。また１ビットあたりの信号エネルギー対雑音電力密度（Ｅｂ／Ｎｏ）は１００ｄＢ、希望波

電力対干渉波電力比（Ｄ／Ｕ）は１００ｄＢであり、雑音と干渉の影響が極めて小さい条件設定をおこなった。なお時間ｔ＝５１２におけるピークは隣接シンボルによるものであり、伝送路のインパルス応答とは無関係である。

【００１５】図５は図４のマッチドフィルタ出力を１６シンボル時間表示したもので、実数成分（Ｉ相）と、虚数成分（Ｑ相）を同時に表示している。従って、ピークが１本しかない場合は、Ｉ相、Ｑ相が同一極性を持ち、ピークが上下に存在するのは、Ｉ相、Ｑ相が互いに逆相となっていることを示している。図から分かるように、このような理想的な条件では明瞭なピークが生じ、他ユーザーによる干渉は生じない。

【００１６】図６はＤ／Ｕ＝－１０ｄＢ、すなわち希望局の他に１０個の干渉局が存在し、（希望波電力）＝０．１×（干渉波電力）の状態を示すシミュレーション結果である。ここではｔ＝０の希望局ピークの他に、ｔ＝２７０の時点で大きな干渉ピークを生じている。この干渉ピークは相互相関値に左右されるため、拡散符号が変われば異なる時点に生じ、誤判定の要因となる。または干渉ピークの存在により希望局ピークレベルが減衰する可能性があり、この点でも誤判定が生じ易い。

【００１７】図７は図６と同一条件における干渉局用のマッチドフィルタ出力であり、図６の希望局ピークよりも明瞭に干渉局ピークが生じている。このピークの位置はｔ＝１２８の時点であるが、これは非同期ＣＤＭＡの方式を採用したことによる。ここに非同期ＣＤＭＡとは、同一セル内において、各ユーザーの拡散符号を非同期としたものである。今回は最悪条件として、干渉波の拡散符号位相を、相互相関値が最悪となる１２８サンプル分（３２チップ分）シフトさせている。

【００１８】図８は図６のマッチドフィルタ出力を１６シンボル期間表示したものである。この場合ｔ＝０に生ずるべき希望局ピークが不安定であり、検出不能である。すなわち相互相関値のレベルによっては希望局が埋もれることもあることが分る。

【００１９】以上のグラフとの比較において、図１の実施例により干渉波を除去した結果を図９に示す。すなわち、図９は図１の実施例により干渉波を除去した結果を示すものであり、希望局のピークが安定し、干渉波が存在しない場合（図５）とほぼ同様の特性が得られている。すなわち干渉波の除去により、希望局ピークを確実に検出し得るようになる。

【００２０】次にマルチパスが生じた場合について説明する。

【００２１】図１０は伝送路のインパルス応答を３パス静的条件したときのマッチドフィルタ出力であり、希望局の直接波がｔ＝１２８に生じ、ｔ＝１３８、ｔ＝１４８に遅延波が生じている。ここに各パスのゲインは１．０、０．７、０．５に設定してある。

【００２２】図１１は図１０のマルチパス信号についてＥｂ／Ｎｏ＝１００ｄＢ（雑音の影響がほとんどない。）、Ｄ／Ｕ＝－１０ｄＢ（干渉波の影響が大きい。）なる条件の下に１６シンボル時間のマッチドフィルタ出力を表示したものである。同図では干渉波レベルが高いために希望局のピークを認識できななっている。

【００２３】図１２は図１１と同一のマルチパス信号に対して図１の実施例による干渉キャンセルを行ったものであり、希望局の直接波が明瞭なピークとなって表れており、確実にピーク検出を行い得ることが分かる。

【００２４】図１３は、種々Ｅｂ／Ｎ０に対するビット誤り率を示し、図１の実施例によるビット誤り率（１点鎖線および丸印プロットで示す。）、何等干渉波キャンセルを行わないときのビット誤り率（破線）、およびビット誤り率理論値（実線）を比較するグラフである。図から干渉波キャンセルを行わないときには、本実施例に比較してビット誤り率が数倍から数１０倍になり、また本実施例は理論値に近似した値となっている。

【００２５】図１の実施例における複素マッチドフィルタＭＦ１１～ＭＦ１ｎ、ＭＦ２１～ＭＦ２ｎ、主波抽出部ＴＨ１１～ＴＨ１ｎ、再拡散部ＲＳ１１～ＲＳ１ｎ、加算器ＡＤＤ１１～ＡＤＤ１ｎ、判定回路Ｊ１１～Ｊ１ｎの処理は以下に例示するように種々の態様により実現可能である。

①全体を汎用コンピュータ上においてソフトウエアで実現した態様。

②ＣＰＵにとっては計算負荷の高いマッチドフィルタのみをＤＳＰあるいは専用のデジタル回路で実現し、その他の部分をソフトウエアにより実現した態様。

③全体をＤＳＰあるいは専用のデジタル回路で実現した態様。

④ＣＰＵにとっては計算負荷の高いマッチドフィルタのみをアナログ回路で実現し、その他の部分をソフトウエアにより実現した態様。

⑤マッチドフィルタのみをアナログ回路で実現し、その他の部分をＤＳＰあるいは専用のデジタル回路で実現した態様。

⑥全体をアナログ回路で実現した態様。

これら態様において、処理速度を高めるためにはアナログまたはデジタルの専用回路の比率を高める必要があり、また消費電力の点でデジタル回路よりもアナログ回路が有利である。

【００２６】図１４は専用デジタル回路によるマッチドフィルタＭＦ１１を示し、図１５は専用デジタル回路による主波抽出部ＴＨ１１を示す。

【００２７】図１４において、マッチドフィルタＭＦ１１はデジタル化された受信信号Ｖｉｎ１４が入力されるｎステージのシフトレジスタＳＦＴＲＥＧを有し、シフトレジスタの各ステージには乗算回路ＭＵＬ１４１～ＭＵＬ１４ｎがそれぞれ接続されている。各乗算回路には

ＰＮ符号が乗数として設定されており、受信信号に対してＰＮ符号を乗ずる演算が行われる。そして乗算回路の出力は全て加算回路ＡＤＤ１４に入力され、ここにおいて積算される。積算結果Ｖｏｕｔ１４はいわゆるマッチドフィルタ出力である。なおＰＮ符号は通常１ビットのデータであるので、乗算回路は入力信号の各ビットを通過させるだけのＡＮＤゲート等で足りる。

【００２８】主波抽出回路ＴＨ１１はマッチドフィルタ出力Ｖｉｎ１５を１シンボル時間分保持するシフトレジスタＳＦＴＲＥＧを有し、このシフトレジスタの各ステージには比較回路Ｃ１～Ｃｎが接続されている。シフトレジスタの初段ステージは最大値回路ＭＡＸに接続され、この最大値回路には後段のマルチプレクサＭＵＸからの帰還データが入力されている。最大値回路ＭＡＸの出力はセレクタＳＥＬを介してレジスタＲＥＧ１またはＲＥＧ２に接続され、マルチプレクサＭＵＸはこれらレジスタの出力を択一的に出力する。最大値回路はＭＵＸから出力されたデータと新たな初段ステージデータとを比較し、より大きいデータを新たなレジスタに入力する。ここに、ＭＵＸから出力されたデータがＲＥＧ１からのものであったときにはＲＥＧ２が新たなレジスタとなり、ＲＥＧ２に対してはＲＥＧ１が新たなレジスタとなる。したがってＲＥＧ１、ＲＥＧ２には交互により大きいデータが登録されることになる。セレクタは常に新たなレジスタに切換えられ、マルチプレクサはこれに呼応して切換えられる。

【００２９】マルチプレクサの出力はさらに乗算回路ＭＵＬに接続され、ここで最大値に所定の比率を掛けた閾値Ｖｔｈが算出される。ここで算出された閾値は比較回路Ｃ１～Ｃｎに入力され、シフトレジスタの各ステージのデータと比較される。その比較結果は図１６に示すとおりであり、Ｖｔｈ以上のデータのみがそのまま出力され、Ｖｔｈ未満のデータは０Ｖに切り捨てられる。これによって前記主波抽出の処理が可能になる。

【００３０】図１７は本発明に係る復調装置の１実施例を示すものであり、主波抽出部、再拡散部および判定回路を専用デジタル回路で実現し、その他を専用アナログ回路で実現している。

【００３１】図１７において、受信信号Ｒ（ｔ）はアナログのマッチドフィルタＭＦ１１～ＭＦ１ｎおよび遅延回路Ｄ１７に入力され、ＭＦ１１～ＭＦ１ｎの出力はＡ／Ｄ変換回路ＡＤＣ１１～ＡＤＣ１ｎを経て、デジタルの主波抽出回路ＴＨ１１～ＴＨ１ｎ、再拡散回路ＲＳ１１～ＲＳ１ｎに入力される。ＲＳ１１～ＲＳ１ｎの出力はＤ／Ａ変換回路ＤＡＣ１１～ＤＡＣ１ｎを経て加算回路ＡＤＤ１１～ＡＤＤ１ｎに入力され、遅延回路Ｄ１７の出力から減算される。加算回路の出力はマッチドフィルタＭＦ２１～ＭＦ２ｎに入力され、その後再度Ａ／Ｄ変換回路ＡＤＣ２１～ＡＤＣ２ｎを経て判定回路Ｊ１１～Ｊ１ｎに入力される。

【００３２】図１８において、アナログのマッチドフィルタＭＦ１１は複数のアナログ遅延回路Ｄ１８１、Ｄ１８２、．．．、Ｄ１８ｎを直列に接続し、アナログの受信信号Ｒ（ｔ）は初段遅延回路から順次後段に転送されて最終段遅延回路Ｄ１８ｎに至る。各遅延回路の出力にはアナログ乗算回路ＭＵＬ１８１、．．．、ＭＵＬ１８ｎが接続され、これら乗算回路においてＰＮ符号ＰＮ１、ＰＮ２、．．．、ＰＮｎが受信信号に掛けられる。乗算回路ＭＵＬ１８１～ＭＵＬ１８ｎの出力は加算回路ＡＤＤ１８１に入力され、全ての乗算結果が加算される。遅延回路Ｄ１８１～Ｄ１８ｎでの遅延時間をＴｃとすると、以上のマッチドフィルタでは以下の演算が実行される。

【数３】

$$S(t)=\sum_{i=1}^{n} PNi \cdot R(t-i \cdot Tc) \qquad (3)$$

なお以上の構成はＭＦ１２～ＭＦ１ｎ、ＭＦ２１～ＭＦ２ｎについても同様である。

【００３３】図１９において、遅延回路Ｄ１７は複数のサンプル・ホールド回路ＳＨ１９１～ＳＨ１９ｎを直列に接続し、初段サンプル・ホールド回路ＳＨ１９１に入力された入力電圧Ｖｉｎ１９を順次後段に転送するもので、各サンプル・ホールド回路はクロックＣＬＫ１９に呼応してデータのサンプル・ホールドを行う。受信信号Ｒ（ｔ）がマッチドフィルタ、主波抽出部、再拡散部を経て加算回路に到達するタイミングに同期するように、遅延回路の段数およびクロックのタイミングが設定されている。なお、遅延回路はシフトレジスタの機能を併せ持ち、各サンプル・ホールド回路からの出力Ｖｏｕｔ１９１～Ｖｏｕｔ１９ｎをそのままデータとして使用することも可能である。なお図１８におけるアナログ遅延回路も図１９と同様の構成になる。

【００３４】サンプル・ホールド回路ＳＨ１９１は図２０のように構成され、バッファＢ２０１、スイッチＳＷ２０１、バッファＢ２０２、スイッチＳＷ２０２、バッファＢ２０３を順次直列に接続し、かつスイッチＳＷ２０１、ＳＷ２０２の後段に接地キャパシタンスＣ２０１、Ｃ２０２を接続してなる。バッファＢ２０１には入力電圧Ｖｉｎ２０が入力され、バッファは後段の負荷にかかわらず安定にＶｉｎ２０を出力する。ＳＷ２０１を閉成した時点で接地キャパシタンスＣ２０１がバッファＢ２０１の出力電圧に対応した電荷に充放電され、キャパシタンスＣ２０１により電圧が保持されることになる。保持完了後にスイッチＳＷ２０１は開放され、次の入力電圧の保持に備える。保持された電圧はバッファＢ２０２の入力電圧となり、バッファＢ２０２から安定に

出力される。ここでスイッチＳＷ２０２を閉成すると、バッファＢ２０２の出力電圧に応じて接地キャパシタンスＣ２０２が充放電され、バッファＢ２０２の出力が保持される。接地キャパシタンスＣ２０２で保持された電圧はバッファＢ２０３の入力電圧となり、バッファＢ２０３の安定な出力Ｖｏｕｔ２０として後段に出力される。

【００３５】スイッチＳＷ２０１、ＳＷ２０２は所定のタイミングで交互に閉成され、入力電圧Ｖｉｎ２０は順次Ｃ２０１、Ｃ２０２に転送、保持される。そしてＣ２０２に転送された電圧は次回のスイッチＳＷ２０２の閉成まで入力電圧Ｖｉｎ２０の影響を受けないので、安定な出力Ｖｏｕｔ２０を生成し得る。

【００３６】バッファＢ２０１としてはヴォルテージフォロワ型（図２１）または反転バッファ型（図２２）等を採用し得る。

【００３７】図２１において、バッファＢ２０１は演算増幅器ＯＰ２１の非反転入力に入力電圧Ｖｉｎ２１を接続し、出力電圧Ｖｏｕｔ２１をその反転入力に帰還させてなる。この回路では入出力の比が＋１となり、入力がそのまま出力に生じる。

【００３８】図２２の回路は、演算増幅器ＯＰ２２の非反転入力を接地し、反転入力にインピーダンスＺ２２１を介して入力電圧Ｖｉｎ２２を接続してなる。また演算増幅器ＯＰ２２の出力はインピーダンスＺ２２１と等しいインピーダンスＺ２２２を介して反転入力に帰還されている。この回路の出力Ｖｏｕｔ２２は－Ｖｉｎ２２に等しく、サンプル・ホールド回路において３段のバッファＢ２０１、Ｂ２０２、Ｂ２０３を介して入力電圧が出力されるため最終出力は反転する。従って、遅延回路におけるサンプル・ホールド回路が偶数段であるときは最終出力Ｖｏｕｔ１９（図１９）はＶｉｎ１９と同一符号となるが、奇数段のときには入力または出力を反転させるためのバッファをさらに付加すべきである。なおサンプル・ホールド回路ＳＨ１９２～ＳＨ１９ｎはＳＨ１９１と同様に構成されているので説明を省略する。

【００３９】図２３はサンプル・ホールド回路の動作を示すグラフであり、ＳＨ１９１、ＳＨ１９２に関して、入力電圧（Ｖｉｎ２０）、２段目バッファ（Ｂ２０２）出力、出力電圧（Ｖｏｕｔ２０）をクロックＣＬＫ２０との関係において表示している。

【００４０】いまＳＨ１９１に対するＶｉｎ２０が変化するなかでスイッチＳＷ２０１が閉成（ＣＬＫ２０は低レベル）されると、閉成された期間中はＶｉｎ２０がそのままＳＨ１９１のＢ２０２出力として表れる。ＳＷ２０１が開放（ＣＬＫ２０は高レベル）された時点でＢ２０２出力は保持され、ＣＬＫ２０が再び低レベルになるまでＢ２０２出力は一定である。スイッチＳＷ２０２はＣＬＫ２０の高レベル時に閉成され、ＳＷ２０１開放時に保持された電圧をＣＬＫ２０の１周期分順次保持した電圧を生成し、Ｖｏｕｔ２０として出力する。

【００４１】サンプル・ホールド回路ＳＨ１９１の出力は第２段目のサンプル・ホールド回路ＳＨ１９２の入力電圧（Ｖｉｎ２０）となり、ＳＨ１９２においては、ＳＷ２０１により入力電圧をＣＬＫ２０の半周期分遅延したタイミングで保持し、さらにＳＷ２０２によりそれをさらに半周期遅延させた電圧を生成して出力電圧Ｖｏｕｔ２０として出力する。

【００４２】以上のアナログタイプの遅延回路はデジタル型の遅延回路に比較して回路規模が小さくかつ消費電力がわずかである。

【００４３】図２４はサンプル・ホールド回路の第２実施例を示す。このサンプル・ホールド回路は３段のＣＭＯＳインバータＩ２４１、Ｉ２４２、Ｉ２４３によって反転バッファと同様の特性を実現したものであり、Ｉ２４３の出力は帰還キャパシタンスＣ２４２を介してＩ２４１の入力に帰還され、Ｉ２４１の入力にはＣＭＯＳスイッチＳＷ２４１、入力キャパシタンスＣ２４１を順次介して入力電圧Ｖｉｎ２４が接続されている。

【００４４】ＳＷ２４１が一旦閉成されてから開放されると、Ｃ２４１はその時点のＶｉｎ２４に応じた電荷に充放電される。Ｃ２４２はＣ２４１と等しく設定され、３段インバータＩ２４１～Ｉ２４３はＣ２４１で保持された電圧をそのままＩ２４３の出力として出力する。Ｉ２４３の出力にはＣＭＯＳスイッチＳＷ２４２が接続され、図２０のサンプル・ホールド回路と同様に、ＳＷ２４１、ＳＷ２４２を交互に開閉することにより、入力電圧の保持、出力が可能である。

【００４５】さらにＳＷ２４２に出力はキャパシタンスＣ２４４を介して上記と同様の３段ＣＭＯＳインバータＩ２４４、Ｉ２４５、Ｉ２４６に入力され、Ｉ２４６の出力は帰還キャパシタンスＣ２４５を介してＩ２４４の入力に接続されている。これによってサンプル・ホールド回路の入出力の符号が整合するようになっている。

【００４６】これら３段インバータは、最終段ＭＯＳインバータの出力にはローパスフィルタとしての接地キャパシダンスＣ２４３、Ｃ２４６が接続され、かつ２段目の出力に１対の平衡レジスタンスＲＥ２４１、ＲＥ２４２、ＲＥ２４３、ＲＥ２４４が接続されている。ＲＥ２４１、ＲＥ２４３は電源電圧Ｖｄｄに接続され、ＲＥ２４２、ＲＥ２４４は接地されており、３段インバータのゲインを抑制している。このような回路構成により、フィードバック系を含む３段インバータの発振が防止されている。

【００４７】図２５は前記マッチドフィルタＭＦ１１の乗算回路を示すものであり、入力電圧Ｖｉｎ２５を複数の異なるインピーダンスＺ２５１、Ｚ２５２、．．．、Ｚ２５ｎに導き、これらインピーダンスの出力をスイッチＳＷ２５１～ＳＷ２５ｎによって任意の組合せで演算増幅器ＯＰ２５の反転入力に入力している。演算増幅器

ＯＰ２５は非反転入力が接地され、かつ出力が帰還インピーダンスＺ２５ｆを介して反転入力に帰還されている。演算増幅器ＯＰ２５は反転バッファを構成し、各イ

$$Z25i = \frac{1}{j\omega C25i}$$

と表現され、スイッチが閉成されたコンデンサの容量の合計をΣＣ２５ｉと表わすと、出力電圧Ｖｏｕｔ２５

$$Vout25 = -\frac{\sum C25i}{C25f} Vin25$$

となる。これはＶｉｎ２５に対して－（Ｃ２５ｉ／Ｃ２５ｆ）を乗じた乗算を意味する。ＳＷ２５１～ＳＷ２５ｎは任意の組合せで閉成され、例えばＣ２５ｉの容量を２のべき乗に設定すれば、２進数の任意の乗数の乗算が可能になる。なおＰＮ符号は（１、０）あるいは（１、－１）の２値のときにはこのような重み付けは不要である。

【００４８】なお式（５）に示すように出力の符号は反転するのでこれをそのまま出力として使用するときにはさらに符号を反転させる反転バッファ等が必要である。また式（５）には係数の符号が含まれていない。図２６はこの反転または符号調整のための付加回路であり、乗数（ＰＮ符号）の符号に応じてＶｏｕｔ２５を反転バッファに導き、あるいは直接出力する。反転バッファは演算増幅器ＯＰ２６の反転入力にインピーダンスＺ２６を

$$Vout27 = -\frac{\sum_{i=1}^{n} Vin27iC27i}{C27f}$$

【００５０】図２８は、（１、０）の２値のＰＮ符号のためのマッチドフィルタＭＦ１１を示し、マッチドフィルタ回路ＭＦ１１は複数（ｎ個）のサンプル・ホールド回路ＳＨ２８１～ＳＨ２８ｎを有し、入力信号Ｖｉｎ２８はこれらサンプル・ホールド回路に並列入力されている。

【００５１】サンプル・ホールド回路ＳＨ２８１は、図２９のように構成され、入力電圧Ｖｉｎ２９はスイッチＳＷ２９に接続されている。スイッチＳＷ２９の出力はキャパシタンスＣ２９１に接続され、キャパシタンスＣ２９１の出力には３段の直列なＭＯＳインバータＩ２９１、Ｉ２９２、Ｉ２９３が接続されている。最終段のＭＯＳインバータＩ２９３の出力Ｖｏ２９は帰還キャパシタンスＣ２９２を介してＩ２９１の入力に接続され、これによってＶｉｎ２９が良好な線形性をもってＩ２９３の出力に生じるようになっている。ＳＷ２９が閉成されると、Ｃ２９１はＶｉｎ２９に対応した電荷で充電され、Ｉ２９１～Ｉ２９３のフィードバック機能により出力の線形特性が保証される。そして、その後スイッチＳＷ２９が開放されたときにサンプル・ホールド回路ＳＨ２８１はＶｉｎ２９を保持することになる。最終段のＩ２９３の出力は接地キャパシタンスＣ２９３を介してグランドに接続され、また第２段のＩ２９２の出力は１対の平衡レジスタンスＲ２９１、ＲＥ２９２を介して電源電圧Ｖｄｄおよびグランドに接続されている。このような構成により、フィードバック系を含む反転増幅回路の発振が防止されている。なおサンプル・ホールド回路ＳＨ２８２～ＳＨ２８ｎはＳＨ２８１と同様に構成されているので説明を省略する。

【００５２】図３０に示すように、前記乗算回路ＭＵＬ１１は２個のマルチプレクサＭＵＸ３０１、ＭＵＸ３０２よりなり、これらマルチプレクサには前記Ｖｏ２９および共通な基準電圧Ｖｒが接続されている。

【００５３】スイッチＳＷ、マルチプレクサＭＵＸ３０１、ＭＵＸ３０２はコントロール信号Ｓ１、Ｓ２、Ｓ３によってコントロールされ、Ｓ１は一旦閉成された後、入力電圧を取り込むべき時点においてＳＷ２９を開放する。Ｓ２、Ｓ３は反転した信号であり、一方のマルチプレクサがＶｏ２９を出力するときには、他方のマルチプレクサはＶｒを出力する。ＭＵＸ３０１、ＭＵＸ３０２

インピーダンスはコンデンサよりなる。ここでインピーダンスＺ２５ｉはコンデンサＣ２５ｉにより、

【数４】

$$(4)$$

は、

【数５】

$$(5)$$

接続するとともに非反転入力を接地し、かつＯＰ２６の出力を反転入力に帰還させている。反転バッファを経由した出力Ｖｏｕｔ２６１は正のＰＮ符号に対応し、直接出力Ｖｏｕｔ２６２は負のＰＮ符号に対応する。

【００４９】図２７はマッチドフィルタＭＦ１１にける加算回路ＡＤＤ１８１を示す。加算回路ＡＤＤ１８１はインピーダンスＺ２７１～Ｚ２７ｎを演算増幅器ＯＰ２７の反転入力に並列に接続するとともに、非反転入力を接地し、さらに演算増幅器ＯＰ２７の出力をインピーダンスＺ２７ｆを介して反転入力に帰還させている。インピーダンスはコンデンサＣ２７ｉ～Ｃ２７ｎ、Ｃ２７ｆよりなり、各インピーダンスへの入力をＶｉｎ２７１～Ｖｉｎ２７ｎ、出力をＶｏｕｔ２７とすると、

【数６】

$$(6)$$

は拡散符号の「１」（ハイレベル）、「－１」（ローレベル）に対応しており、ある時点の入力電圧に符号「１」を乗ずるべきときには、ＭＵＸ３０１からＶｏ２９を出力し、「－１」を乗ずるべきときにはＭＵＸ３０２からＶｏ２９を出力する。このハイ、ローのレベルを代表するために図３０ではＭＵＸ３０１の出力をＶＨ、ＭＵＸ３０２の出力をＶＬで表示する。

【００５４】図３１に示すように、スイッチＳＷ２９はｎ型ＭＯＳトランジスタのソース、ドレインをｐ型ＭＯＳトランジスタのドレイン、ソースとそれぞれ接続してなるトランジスタ回路Ｔ３１よりなり、このトランジスタ回路のｎＭＯＳのドレイン側の端子に入力電圧Ｖｉｎ３１を接続し、ｎＭＯＳのソースの端子を同様の構成のダミートランジスタＤＴ３１を介して出力端子Ｖｏｕｔ３１に接続してなる。トランジスタ回路Ｔ３１におけるｎＭＯＳトランジスタのゲートにはＳ１が入力され、ｐＭＯＳトランジスタのゲートにはＳ１をインバータＩ３１で反転した信号が入力されている。これによって、Ｓ１がハイレベルのときには、Ｔ３１が導通し、ローレベルのときにはＴ３１は遮断される。

【００５５】図３２に示すように、マルチプレクサＭＵＸ３０１はｎ型、ｐ型の１対のＭＯＳトランジスタのドレイン、ソースを相互に接続してなるトランジスタ回路Ｔ３２１、Ｔ３２２のｎＭＯＳのソース側の端子を共通出力端子Ｖｏｕｔ３２に接続してなり、Ｔ３２１におけるｎＭＯＳのドレイン側の端子にはＭＯＳインバータＩ２９３の出力Ｖｏ２９（図中Ｖｉｎ３２１で示す。）を接続し、Ｔ３２２のドレインには基準電圧Ｖｒ（図中Ｖｉｎ３２２で示す。）が接続されている。トランジスタ回路Ｔ３２１におけるｎＭＯＳトランジスタのゲートおよびトランジスタ回路Ｔ３２２におけるｐＭＯＳトランジスタのゲートには信号Ｓ２が入力され、Ｔ３２１のｐＭＯＳおよびＴ３２２のｎＭＯＳのゲートにはＳ２をインバータＩ３２で反転した信号が入力されている。これによって、Ｓ２がハイレベルのときには、Ｔ３２１が導通してＴ３２２は遮断され、ローレベルのときにはＴ３２２が導通しＴ３２１が遮断される。すなわちＭＵＸ３０１は、Ｓ２のコントロールによりＶｏ２９またはＶｒを択一的に出力し得る。

【００５６】図示は省略するが、マルチプレクサＭＵＸ３０２はＭＵＸ３０１と同様に構成されＶｏ２９とＶｒの接続が逆転している。すなわち、ＶｒをＴ３２１に、Ｖｏ３をＴ３２２に接続した構成となっている。これによって、ＭＵＸ３０２はＭＵＸ３０１と反対の出力、すなわちＭＵＸ３０１がＶｏ２９を出力するときにはＶｒを、ＭＵＸ３０１がＶｒを出力するときにはＶｏ２９を出力する。

【００５７】信号Ｓ２は拡散符号に対応し、乗算回路ＭＵＬ１１はＳ２が「１」のときにはＭＵＸ３０１からＶｏ２９、ＭＵＸ３０２からＶｒを、Ｓ２が「０」のときにはＭＵＸ３０１からＶｒ、ＭＵＸ３０２からＶｏ２９を出力する。これら出力は前記加算回路ＡＤＤ２８に導かれている。すなわち図２８ではＭＵＬ２８１からＡＤＤ２８への信号は１ラインのみ記されているが、これは高レベル側と低レベル側の２系統の信号を代表している。

【００５８】図３３において、加算回路ＡＤＤ２８は、ＭＵＬ２８１、ＭＵＬ２８２、．．．、ＭＵＬ２８ｎからのハイレベル信号ＶＨ１～ＶＨｎが入力された容量結合ＣＰＨ、ＭＵＬ２８１～ＭＵＬ２８ｎからのローレベル信号ＶＬ１～ＶＬｎが入力された容量結合ＣＰＬを有し、ＣＰＬはキャパシタンスＣＬ１～ＣＬｎを並列接続してなり、ＣＰＨはキャパシタンスＣＨ１～ＣＨｎを並列接続してなる。ＣＰＬの出力は３段直列のＭＯＳインバータＩ３３１、Ｉ３３２、Ｉ３３３の初段入力に接続され、Ｉ３３３の出力は帰還キャパシタンスＣ３３１を介して初段入力にフィードバックされている。この３段インバータはその充分大きな開ループ・ゲインによって、入出力関係の線形性を保証している。

【００５９】ＣＰＨの出力は３段直列のＭＯＳインバータＩ３３４、Ｉ３３５、Ｉ３３６の初段入力に接続され、Ｉ３３６の出力は帰還キャパシタンスＣ３３３を介して初段入力にフィードバックされている。この３段インバータはその充分大きな開ループ・ゲインによって、入出力関係の線形性を保証している。さらにＩ３３３の出力は、容量結合ＣＰＨと並列な結合キャパシタンスＣＣ３３を介してＩ３３４の入力に接続され、ＣＰＬの出力の反転とＣＰＨの出力との和が３段インバータＩ３３４～Ｉ３３６に入力されている。

【００６０】前記３段インバータにおける最終段のＭＯＳインバータＩ３３３、Ｉ３３６の出力は接地キャパシタンスＣ３３２、Ｃ３３４をそれぞれ介してグランドに接続され、また第２段のＭＯＳインバータＩ３３２、Ｉ３３５の出力は１対の平衡レジスタンスＲ３３１、Ｒ３３２、Ｒ３３３、Ｒ３３４をそれぞれ介して電源電圧Ｖｄｄおよびグランドに接続されている。このような構成により、フィードバック系を含む反転増幅回路の発振が防止されている。

【００６１】加算回路ＡＤＤ２８は式（７）の演算を実行し、キャパシタンス相互の関係が式（８）～（１０）のように設定されているため、結果的に式（１１）演算結果が得られる。

【数７】

$$Vout33 = Vdd - \frac{\left(Vdd - \frac{\sum_{i=1}^{n} VLi \cdot CLi}{C331} \right) \cdot CC33 + \sum_{i=1}^{n} VHi \cdot CHi}{C333} \quad (7)$$

$$CL1 = CL2 = \ldots = CLn \quad (8)$$

$$CH1 = CH2 = \ldots = CHn \quad (9)$$

$$C331 = C333 = CC33 = n \cdot CLi = n \cdot CHi \quad (10)$$

$$Vout33 = \frac{\sum_{i=1}^{n} (VLi - VHi)}{n} \quad (11)$$

【０００６２】ここでＶＬｉ、Ｖｈｉを基準電圧Ｖｒを基準とした式（１２）、（１３）の表現に改める。

【数８】

$$VHi = Vr + vhi \quad (12)$$

$$VLi = Vr + vli \quad (13)$$

この式（１２）、（１３）を式（１１）に代入すると式（１４）が得られる。

【数９】

$$Vout33 = \frac{\sum_{i=1}^{n} (vli - vhi)}{n} \quad (14)$$

【０００６３】さらに、サンプル・ホールド回路においても３段インバータによるデータの反転が行われているので、ある時刻をｔ、チップ時間をＴｃ、自然数ｉとするとき、入力信号Ｖｉｎ１をサンプル・ホールド回路ＳＨ３１～ＳＨ３ｎによって時系列に保持した信号はＳ（ｔ－ｉ・Ｔｃ）、これに乗ずるＰＮ符号をＰｎｉとするとき、式（１４）は式（１５）に書き換えられる。

【数１０】

$$Vout33 = \frac{\sum_{i=1}^{n} PNi \cdot S(t - i \cdot Tc)}{n} \quad (15)$$

これは一般的なマッチドフィルタの演算である。

【０００６４】なお、以上の演算において出力は入力の個数ｎによって正規化されているため、出力の最大電圧が電源電圧を超えることが防止され、動作の安定性が保証されている。

【０００６５】前記基準電圧Ｖｒは、図３４に示す基準電圧生成回路Ｖｒｅｆによって生成される。この基準電圧生成回路は３段の直列なインバータＩ３４１、Ｉ３４２、Ｉ３４３の最終段出力を初段入力に帰還させた回路であり、前記加算部と同様に接地キャパシタンスＣ３４、平衡レジスタンスＲ３４１、Ｒ３４２による発振防止処理が施されている。基準電圧生成回路Ｖｒｅｆはその入出力電圧が等しくなる安定点に出力が収束し、各ＭＯＳインバータの閾値設定により所望の基準電圧を生成し得る。一般には正負両方向に充分大きなダイナミックレンジを確保するために、Ｖｒ＝Ｖｄｄ／２と設定されることが多い。ここにＶｄｄはＭＯＳインバータの電源電圧である。

【０００６６】図３５はマルチユーザ復調装置の第２実施例を示し、図１７よりもアナログ回路の比率を高め、主波抽出回路、再拡散回路をさらにアナログ化している。

【０００６７】図３６はアナログ型の主波抽出回路ＴＨ１１の第１実施例を示す。主波抽出回路ＴＨ１１はコンパレータＣＭＰ３６よりなり、その入力には入力電圧Ｖｉｎ３６および閾値電圧Ｖｔｈが入力されている。ＣＭＰ３６には高レベルの電圧Ｖ１と低レベルの電圧Ｖ２とが印加され、Ｖｉｎ３６≧Ｖｔｈのときには Ｖ１が、Ｖｉｎ３６＜Ｖｔｈのときには Ｖ２がＣＭＰ３６の出力となる。図３７はＣＭＰ３６の入出力関係を示すグラフであり、入力電圧ＶｉｎがＶｔｈを越えるか否かによって出力電圧Ｖｏｕｔ３６はＶ１からＶ２に急激に変化している。これによって、マッチドフィルタ出力において閾値電圧をこえた部分はＶ１となり、その他の部分はＶ２となる。図２のマッチドフィルタ出力を以上の主波抽出回路によって処理した結果は図３８のとおりとなり、希望波電力が抽出されていることが分る。なおＴＨ１２～ＴＨ１ｎを同様に構成し得ることはいうまでもない。

【０００６８】図３９は主波抽出回路ＴＨ１１の第２実施

例を示す。主波抽出回路ＴＨ１１は入力電圧および前記基準電圧Ｖｒｅｆが入力されたマルチプレクサＭＵＸ３９を有し、マルチプレクサのコントロール信号としてＶｉｎ３９から閾値電圧Ｖｔｈを減算した結果の信号が使用されている。Ｖｔｈはキャパシタンス Ｃ３９１を介して反転バッファとしての３段インバータＩ３９１、Ｉ３９２、Ｉ３９３に入力され、Ｉ３９３の出力はキャパシタンスＣ３９２を介してＩ３９１の入力に帰還されている。またＩ３９３出力には接地キャパシタンスＣ３９３が接続され、Ｉ３９２出力には平衡レジスタンスＲＥ３９１、ＲＥ３９２が接続されている。Ｉ３９３出力およびＶｉｎ３６は、キャパシタンスＣ３９４、Ｃ３９５よりなる容量結合ＣＰ３９に入力され、ＣＰ３９の出力はインバータＩ３９４に入力されている。前記３段インバータはＶｔｈの反転出力を良好な線形特性をもって生成し、容量結合ＣＰ３９はＩ３９３の出力とＶｉｎ３９との和を生成する。ここで、ＣＰ３９の出力をＶｏ３９、Ｃ３９４＝Ｃ３９５とすると、となる。

【数１１】

$$Vo39 = \frac{C394(Vdd - Vth) + C395 \cdot Vin39}{C394 + C395} = \frac{Vdd}{2} + \frac{Vin39 - Vth}{2} \qquad (16)$$

【００６９】インバータＩ３９４はＶｄｄ／２以上の電圧が入力されたとき、すなわちＶｉｎ３９≧Ｖｔｈのときに０Ｖを出力し、Ｖｉｎ３９＜Ｖｔｈのときに Ｖｄｄを出力する。この２値の信号によりＭＵＸ３９が制御される。ＭＵＸ３９はＶｉｎ３９≧Ｖｔｈのときに Ｖｉｎ３９を出力し、Ｖｉｎ３９＜Ｖｔｈのときに Ｖｒｅｆを出力する。従って図２のマッチドフィルタ出力を主波抽出回路によって処理した結果は図４０のとおりである。なおＴＨ１２～ＴＨ１ｎをＴＨ１１と同様に構成し得ることはいうまでもない。

【００７０】図４１は再拡散回路ＲＳ１１の第１実施例を示す。ＲＳ１１において、入力電圧Ｖｉｎ４１がスイッチＳＷ４１に接続され、ＳＷ４１は適当なタイミングにおいてコントロール信号ＣＴＲＬ４１により開閉される。ＳＷ４１の出力はキャパシタンスＣ４１１を介して反転バッファとしての３段インバータＩ４１１、Ｉ４１２、Ｉ４１３に入力され、この３段インバータの出力はキャパシタンスＣ４１４を介して同様の３段インバータＩ４１４、Ｉ４１５、Ｉ４１６に入力されている。Ｉ４１３の出力はキャパシタンスＣ４１２を介してＩ４１１の入力に帰還され、Ｉ４１６の出力はキャパシタンスＣ４１５を介してＩ４１４の入力に帰還されている。Ｉ４１３、Ｉ４１６の出力には接地キャパシタンスＣ４１３、Ｃ４１６がそれぞれ接続され、Ｉ４１２、Ｉ４１５の出力には平衡レジスタンスＲＥ４１１、ＲＥ４１２、ＲＥ４１３、ＲＥ４１４が接続されている。

【００７１】Ｉ４１３、Ｉ４１６の出力はマルチプレクサＭＵＸ４１に入力され、ＭＵＸ４１は２値のＰＮ符号によって切換え制御されている。ＰＮ符号が「１」のときにはＩ４１６の出力が選択され、２段階の反転バッファを経た非反転のＶｉｎ４１がＭＵＸ４１から出力される。またＰＮ符号が「－１」または「０」のときにはＩ４１３の出力が選択され、１段階の反転バッファを経たＶｉｎ４１の反転信号がＭＵＸ４１から出力される。ＭＵＸ４１の出力Ｖｏｕｔ４１は入力電圧Ｖｉｎ４１にＰＮ符号を乗じた結果と等価であり、これはＶｉｎ４１の拡散信号となる。なおＲＳ１２～ＲＳ１ｎはＲＳ１１と同様であるので説明を省略する。

【００７２】図４２は再拡散回路ＲＳ１１の第２実施例を示すものであり、図２０と同様のサンプル・ホールド回路ＳＨ１９１の後段に図２６と同様の回路を接続してなる。サンプル・ホールド回路は、バッファＢ４２１、スイッチＳＷ４２１、バッファＢ４２２、スイッチＳＷ４２２、バッファＢ４２３を直列接続し、ＳＷ４２１、ＳＷ４２２の出力に接地キャパシタンスＣ４２１、Ｃ４２２を接続してなる。Ｂ４２３の出力は１入力２出力のスイッチＳＷ４２３に接続され、その第１の出力は、インピーダンスＣ４２３、演算増幅器ＯＰ４２、帰還キャパシタンスＣ４２よりなる反転バッファに入力されている。この反転バッファの出力はＶｏｕｔ４２１である。またＳＷ２４３の第２の出力はそのまま出力Ｖｏｕｔ４２２とされている。これによって入力電圧Ｖｉｎ４２は、一旦サンプル・ホールド回路によって保持された後、適当なタイミングにおいて、反転バッファによって反転され、あるいは反転されずに出力される。

【００７３】

【発明の効果】前述のとおり、本発明に係るマルチユーザ復調方法は、受信信号を逆拡散した信号を単に閾値処理することによって特定ユーザーの信号を抽出し、抽出された信号を再拡散し、特定ユーザー以外の再拡散信号を受信信号から減ずることにより特定ユーザーのための受信信号を抽出するので、従来同期に関連した問題点を解消し、かつ干渉キャンセラが不要であるという優れた効果を有する。

【図面の簡単な説明】

【図１】本発明方法の１実施例を実施するための装置の概念を示すブロック図である。

【図２】同実施例におけるマッチドフィルタ出力を示すグラフである。

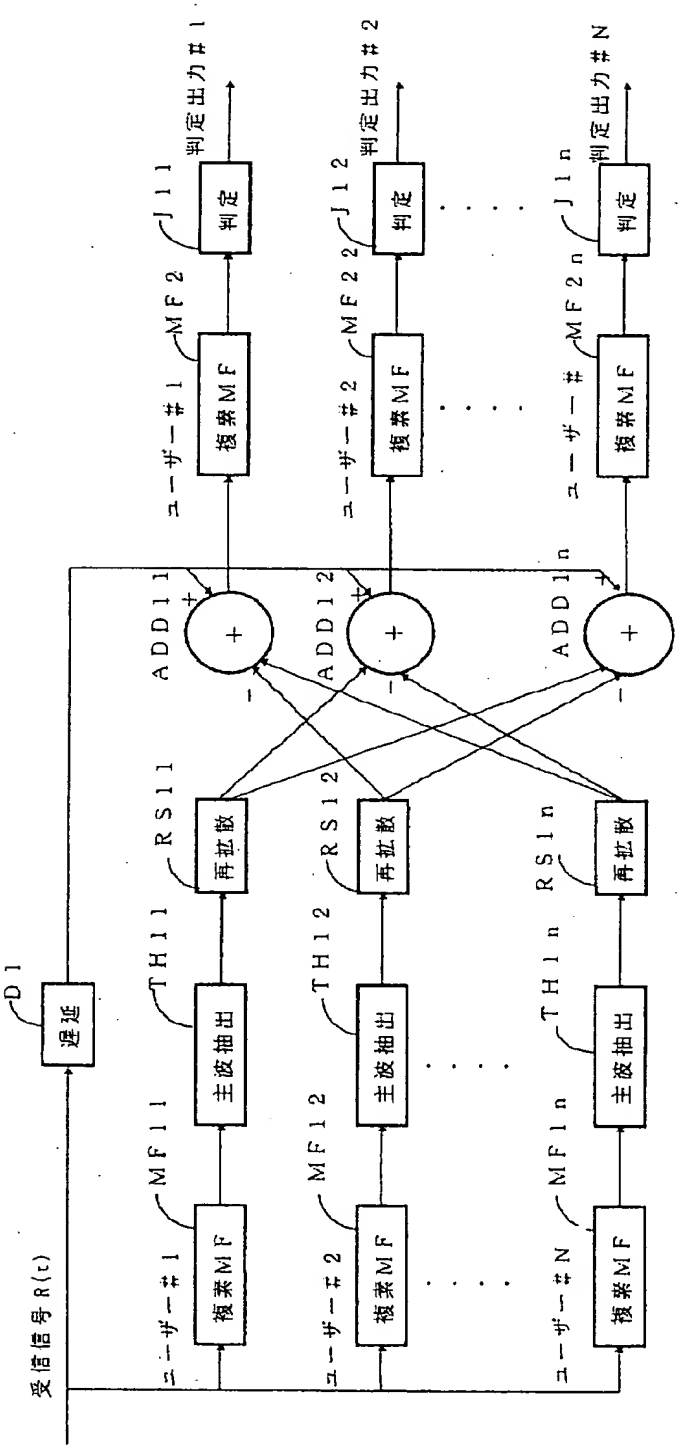
【図３】希望波電力を示すグラフである。

【図４】干渉が少ないときのマッチドフィルタ出力を示すグラフである。

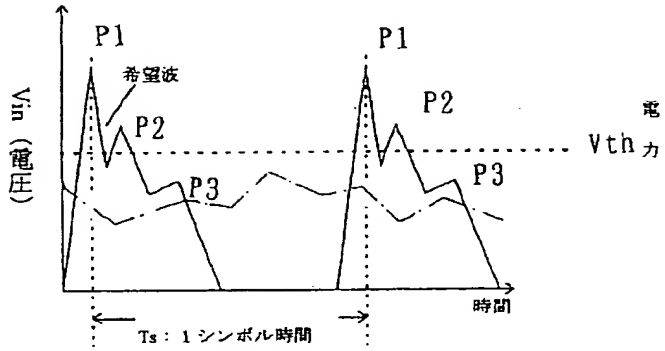
【図５】図４と同一条件においてより長い期間のマッチドフィルタ出力を示すグラフである。

【図６】干渉局の存在下でのマッチドフィルタ出力を示すグラフである。
【図７】図６と同一条件での干渉局用のマッチドフィルタ出力を示すグラフである。
【図８】図６と同一条件においてより長い期間のマッチドフィルタ出力を示すグラフである。
【図９】図６と同一の受信信号に対して図１の実施例により干渉波を除去した後のマッチドフィルタ出力を示すグラフである。
【図１０】マルチパス信号のマッチドフィルタ出力である。
【図１１】図１０と同一のマルチパス信号に干渉波の影響を加えたときのマッチドフィルタ出力である。
【図１２】図１１と同一の受信信号に対して図１の実施例により干渉波を除去した後のマッチドフィルタ出力を示すグラフである。
【図１３】図１の実施例によるビット誤り率を、干渉波除去を行わないときおよび理論値と比較するグラフである。
【図１４】専用デジタル回路によるマッチドフィルタの１実施例を示すブロック図である。
【図１５】専用デジタル回路による主波抽出回路の１実施例を示すブロック図である。
【図１６】主波抽出回路の出力を示すグラフである。
【図１７】マッチドフィルタをアナログ回路とした復調装置を示すブロック図である。
【図１８】図１７におけるマッチドフィルタを示すブロック図である。
【図１９】図１７における遅延回路を示すブロック図である。
【図２０】図１９におけるサンプル・ホールド回路を示す回路図である。
【図２１】図２０におけるバッファの第１実施例を示す回路図である。
【図２２】図２０におけるバッファの第２実施例を示す回路図である。
【図２３】図１９における第１段および第２段のサンプル・ホールド回路の動作を示すタイミングチャートである。
【図２４】サンプル・ホールド回路の第２実施例を示す回路図である。
【図２５】図１８のマッチドフィルタにおける乗算回路を示す回路図である。
【図２６】同マッチドフィルタにおいて正負符号の処理を行うための回路を示す回路図である。
【図２７】同マッチドフィルタにおける加算回路を示す回路図である。
【図２８】アナログ型マッチドフィルタの第２実施例を示すブロック図である。
【図２９】図２８のサンプル・ホールド回路を示す回路図である。
【図３０】図２８の乗算回路を示す回路図である。
【図３１】図２９のスイッチを示す回路図である。
【図３２】図３０のマルチプレクサを示す回路図である。
【図３３】図２８の加算回路を示す回路図である。
【図３４】図３０の基準電圧を生成するための回路を示す回路図である。
【図３５】復調装置の第２実施例を示すブロック図である。
【図３６】アナログ型の主波抽出回路の第１実施例を示す回路図である。
【図３７】同主波抽出回路の入出力特性を示すグラフである。
【図３８】図２のマッチドフィルタ出力を同主波抽出回路で処理した結果を示すグラフである。
【図３９】アナログ型の主波抽出回路の第２実施例を示す回路図である。
【図４０】図２のマッチドフィルタ出力を同主波抽出回路で処理した結果を示すグラフである。
【図４１】再拡散回路の第１実施例を示す回路図である。
【図４２】再拡散回路の第２実施例を示す回路図である。
【符号の説明】
ＡＤＤ１１、．．．、ＡＤＤ１ｎ、ＡＤＤ１８１
．．．加算回路
ＡＤＣ１１、．．．、ＡＤＣ１ｎ、ＡＤＣ２
１、．．．、ＡＤＣ２ｎ　．．．Ａ／Ｄコンバータ
Ｂ２０１、Ｂ２０３、Ｂ２０３　．．．バッファ
ＤＡＣ１１、．．．、ＤＡＣ１ｎ　．．．Ｄ／Ａコンバータ
Ｄ　．．．遅延回路
Ｄ１８１、．．．、Ｄ１８ｎ　．．．遅延回路
Ｊ１１、．．．、Ｊ１ｎ　．．．判断回路
ＭＦ１１、．．．、ＭＦ１ｎ　．．．マッチドフィルタ
ＭＦ２１、．．．、ＭＦ２ｎ　．．．マッチドフィルタ
ＭＵＬ１８１、．．．、ＭＵＬ１８ｎ　．．．乗算回路
ＯＰ２１、ＯＰ２２、ＯＰ２５、ＯＰ２６、ＯＰ２７
．．．演算増幅回路
Ｐ１、Ｐ２、Ｐ３　．．．ピーク
Ｒ（ｔ）　．．．入力信号
ＲＳ１１、．．．、ＲＳ１ｎ　．．．再拡散回路
ＳＨ１９１、．．．、ＳＨ１９ｎ　．．．サンプル・ホールド回路
Ｖｔｈ　．．．閾値電圧。
8

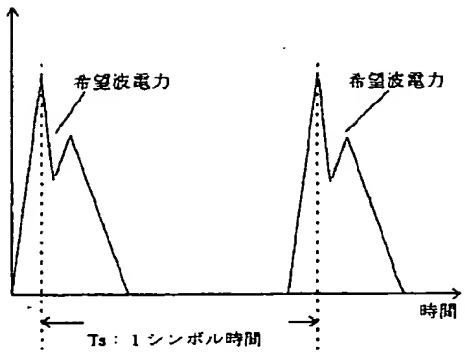
【図１】


受信信号 R(t)
D 1
遅延
ユーザー＃１
ユーザー＃２
ユーザー＃Ｎ
ＭＦ１１
ＭＦ１２
ＭＦ１ｎ
複素ＭＦ
主波抽出
ＴＨ１１
ＴＨ１２
ＴＨ１ｎ
ＲＳ１１
ＲＳ１２
ＲＳ１ｎ
再拡散
ＡＤＤ１１
ＡＤＤ１２
ＡＤＤ１ｎ
＋
－
ＭＦ２１
ＭＦ２２
ＭＦ２ｎ
Ｊ１１
Ｊ１２
Ｊ１ｎ
判定
判定出力＃１
判定出力＃２
判定出力＃Ｎ

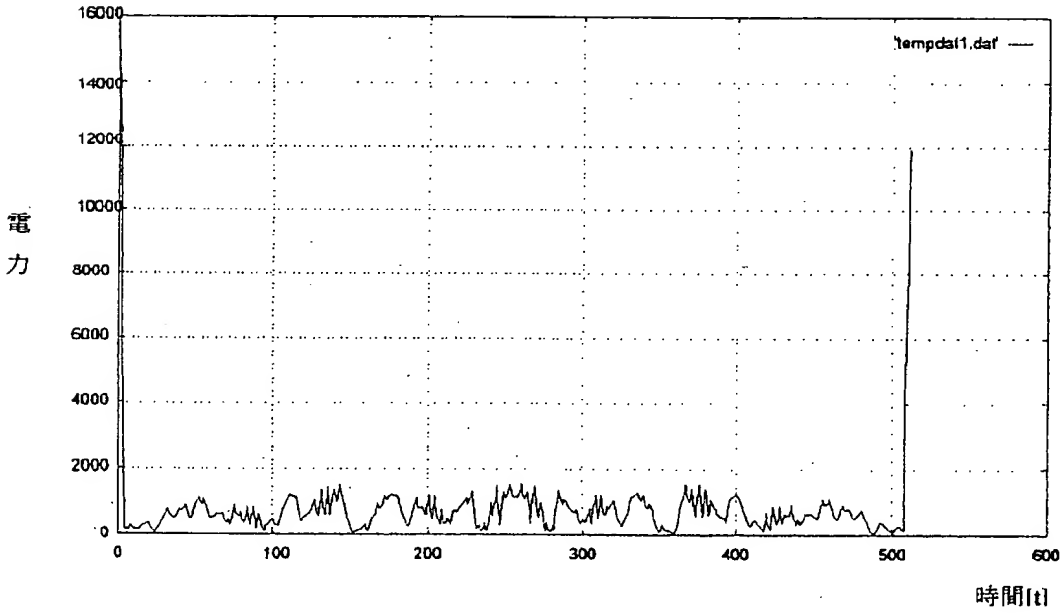
【図２】



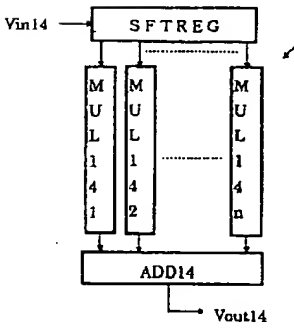
【図３】



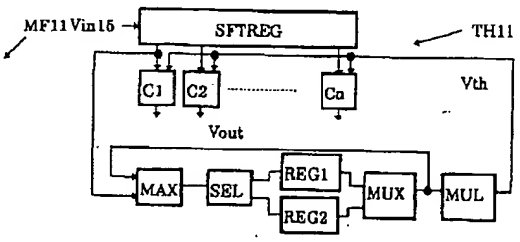
【図４】



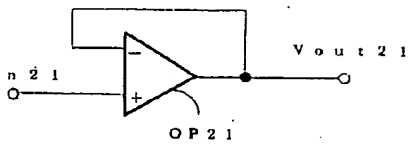
【図１４】



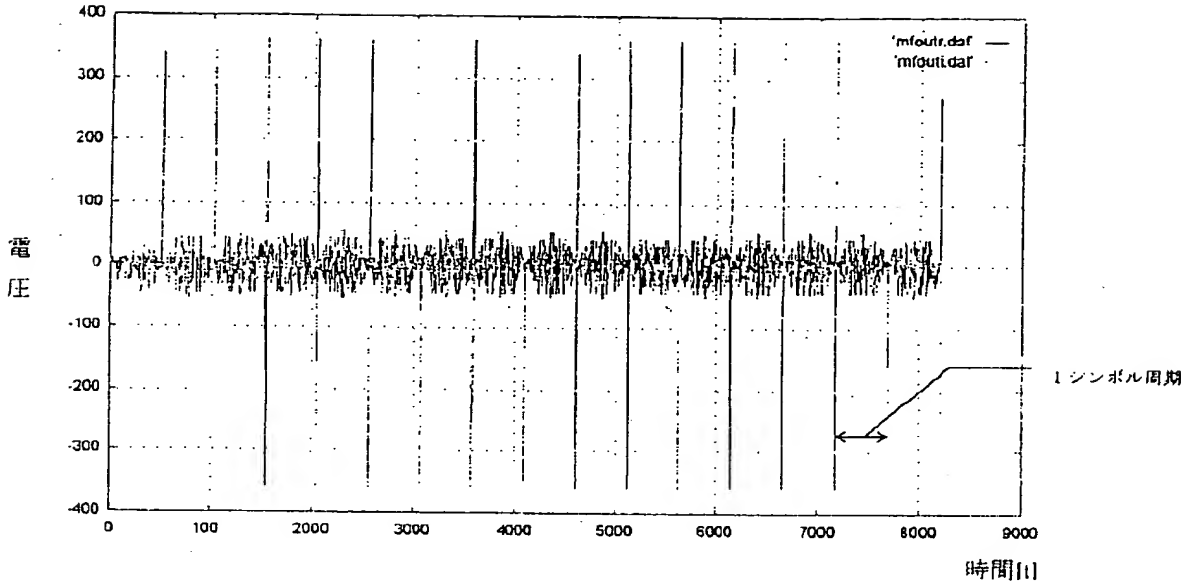
【図１５】



【図２１】



【図５】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300
200
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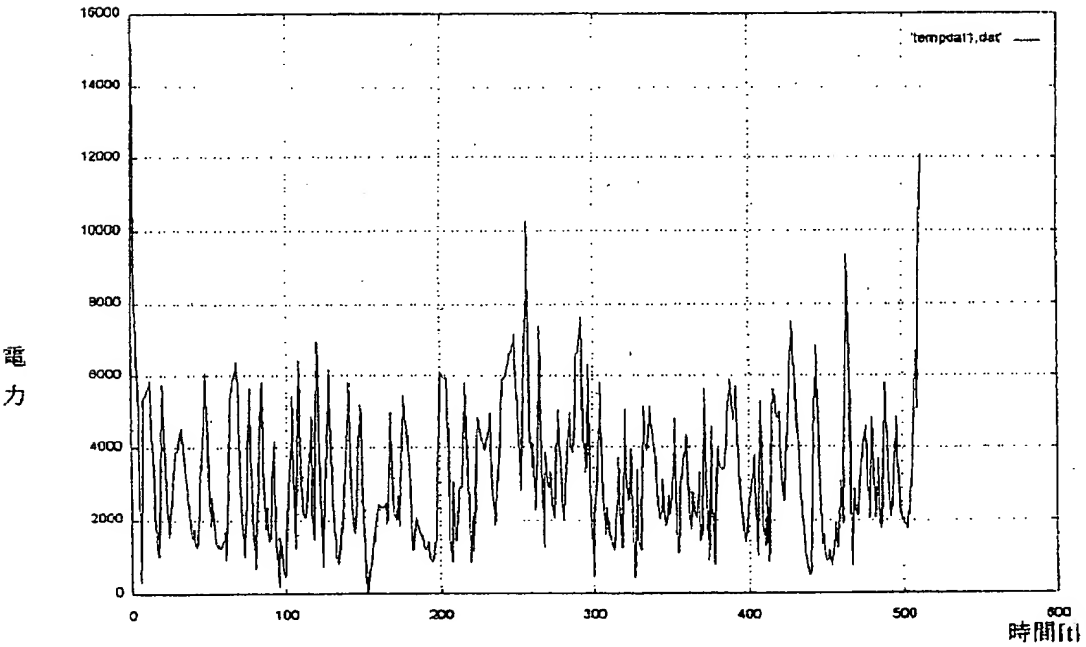
0
-100
-200
-300
-400
0
100
2000
3000
4000
5000
6000
7000
8000
9000
時間[t]
1シンボル周期

【図６】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12000
10000
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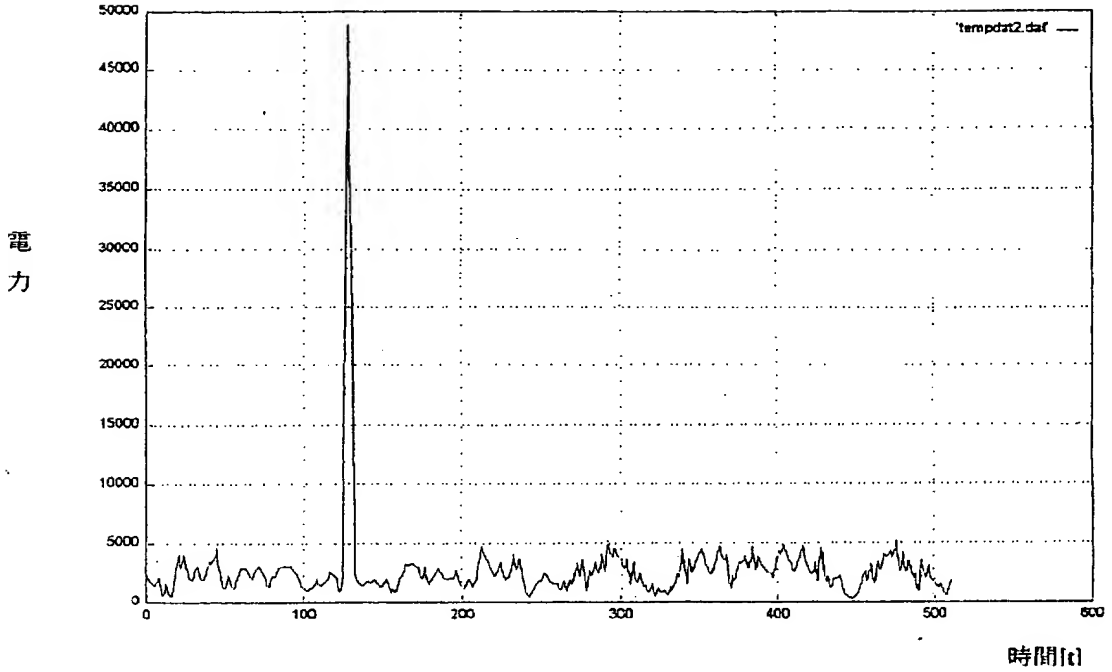
0
0
100
200
300
400
500
600
時間[t]

【図７】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電力
時間[t]

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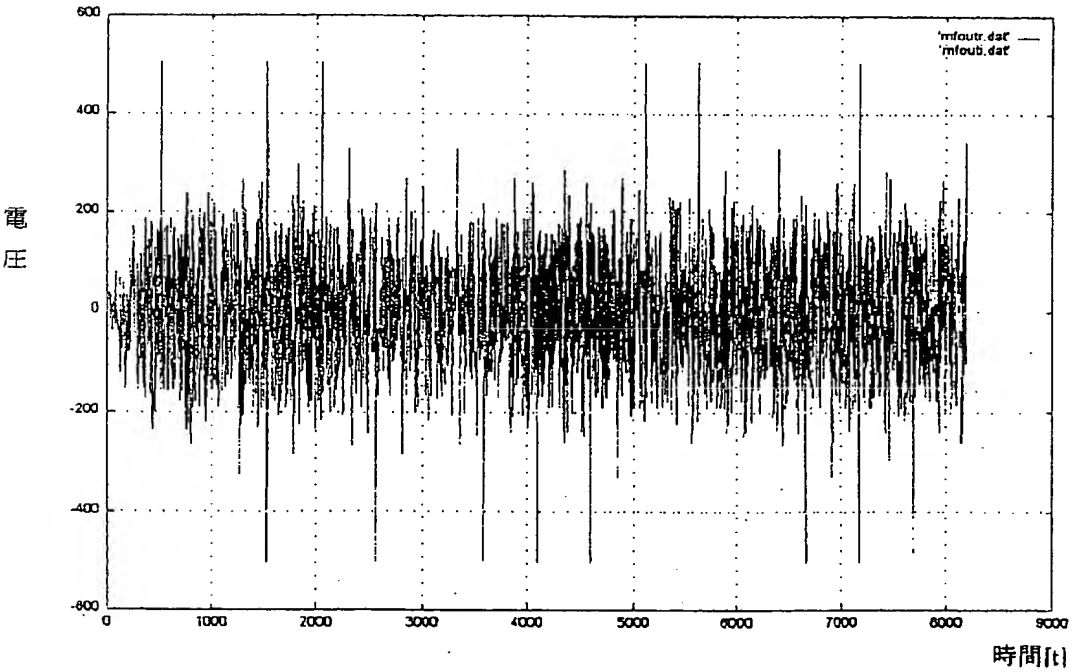
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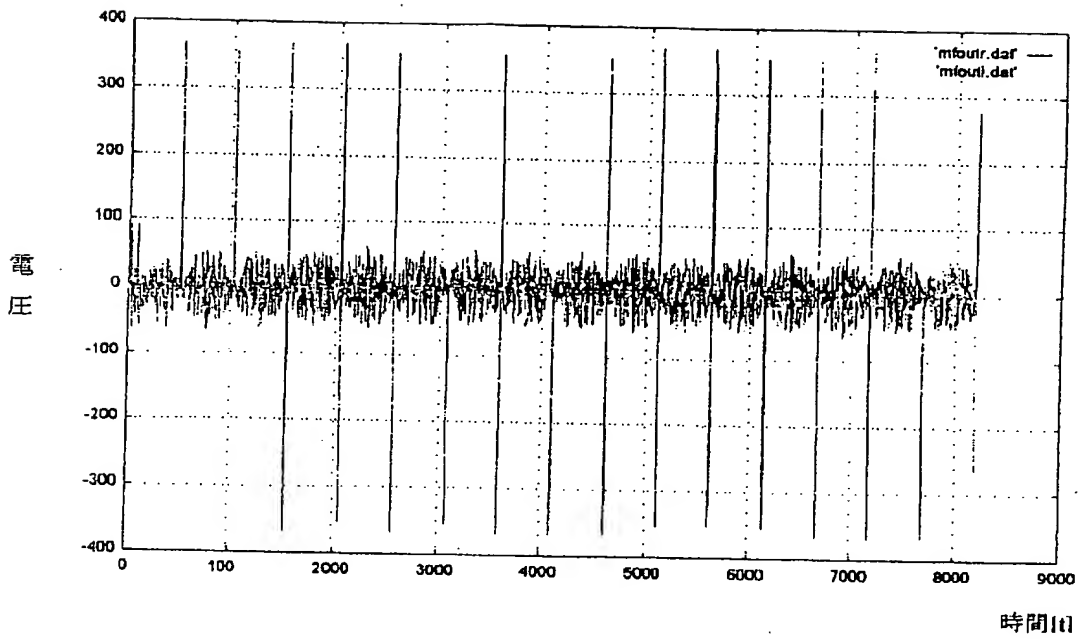

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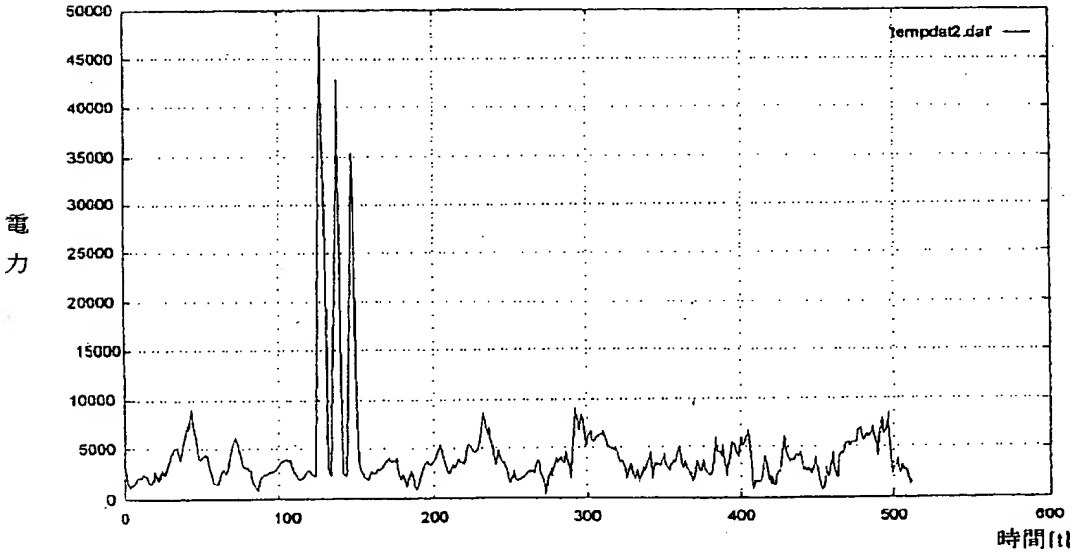

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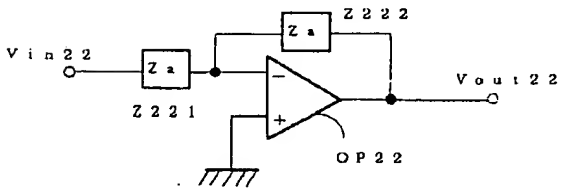

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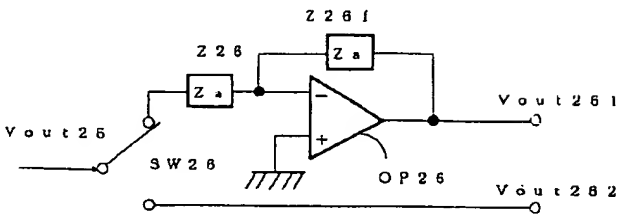

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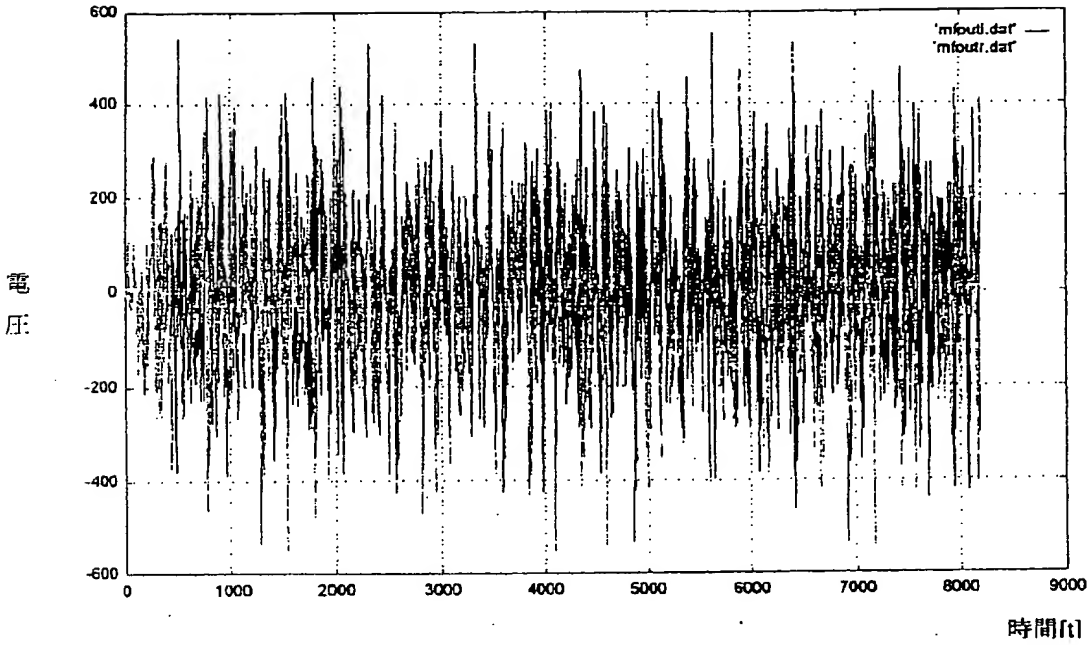

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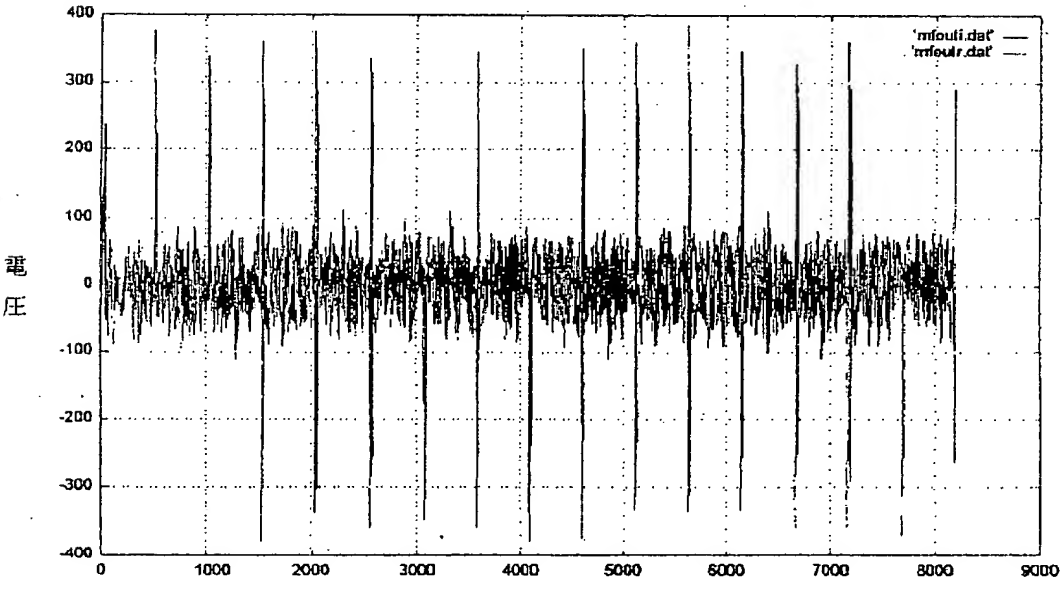

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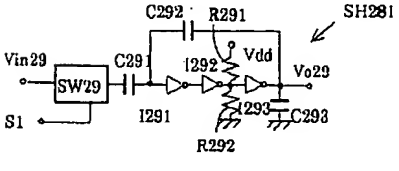

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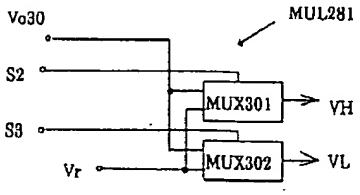

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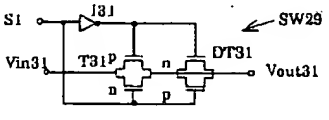

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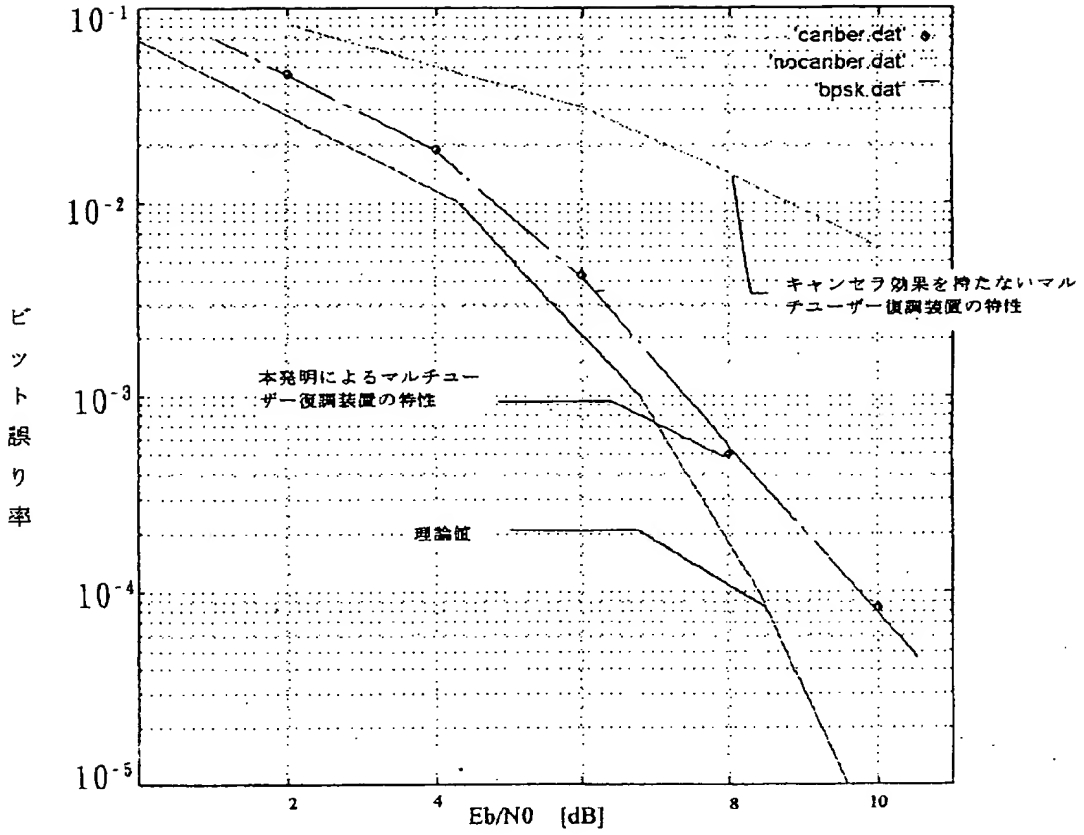

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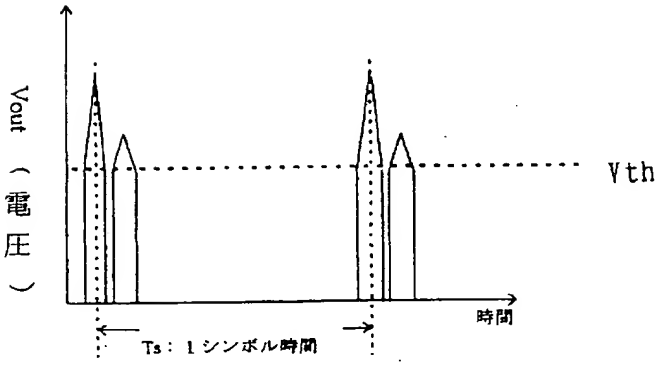

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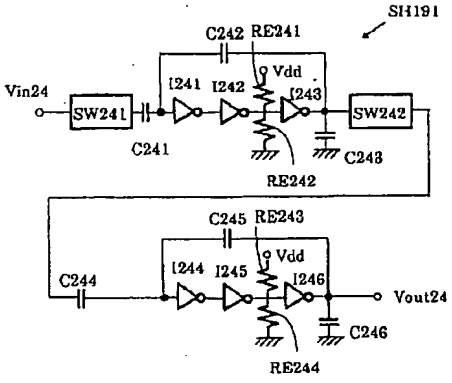

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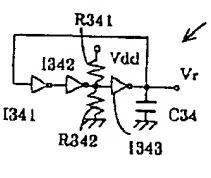

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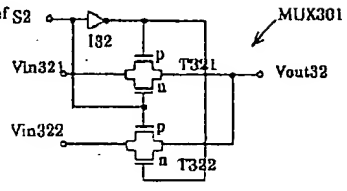

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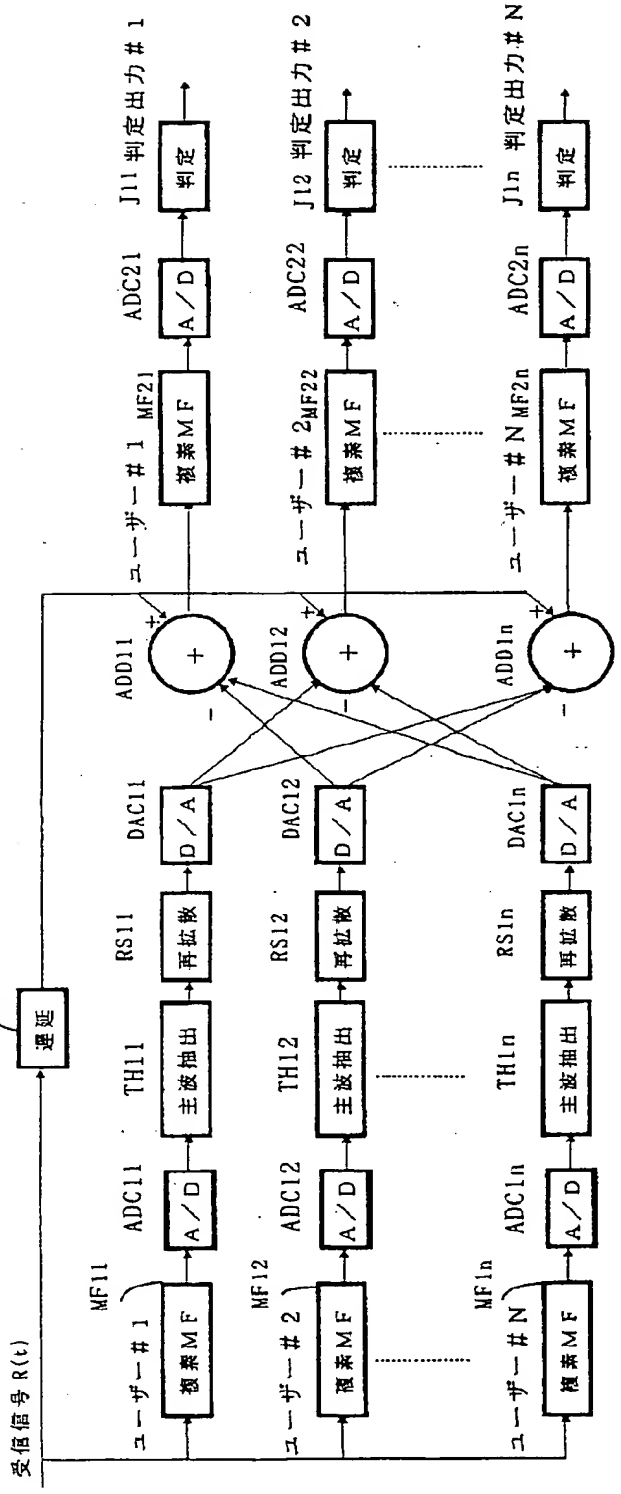
受信信号 R(t)
D17
遅延
ユーザー＃１
ユーザー＃２
ユーザー＃Ｎ
整合ＭＦ
MF11
MF12
MF1n
A／D
ADC11
ADC12
ADC1n
主波抽出
TH11
TH12
TH1n
再拡散
RS11
RS12
RS1n
D／A
DAC11
DAC12
DAC1n
ADD11
ADD12
ADD1n
ユーザー＃１ MF21
ユーザー＃２ MF22
ユーザー＃Ｎ MF2n
ADC21
ADC22
ADC2n
判定
J11 判定出力＃１
J12 判定出力＃２
J1n 判定出力＃Ｎ

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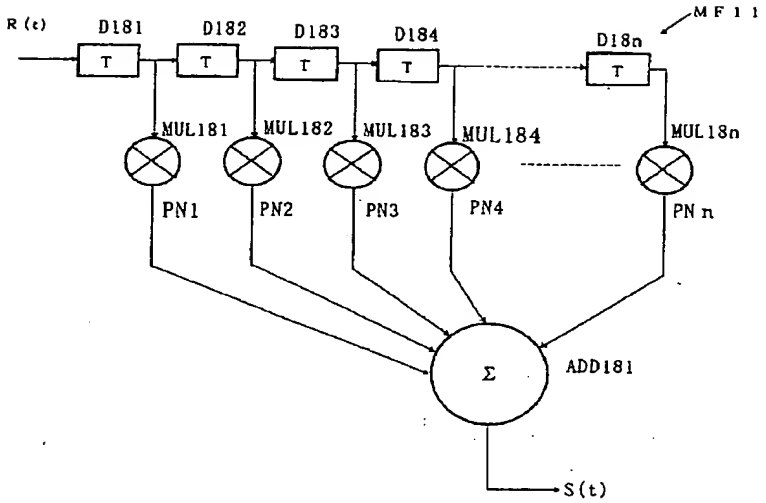

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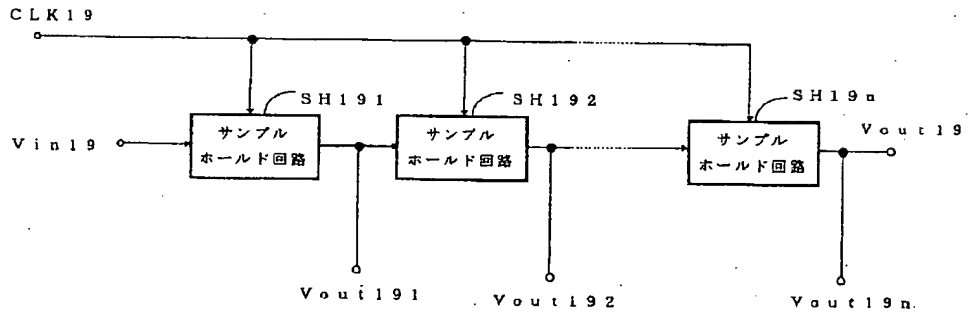

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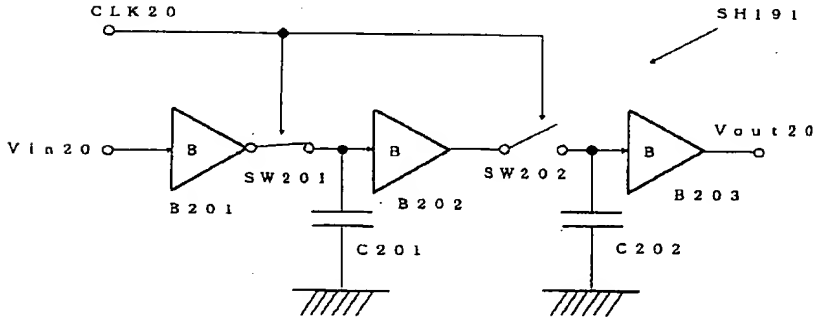

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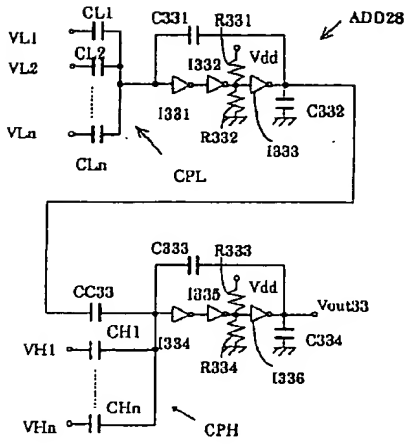

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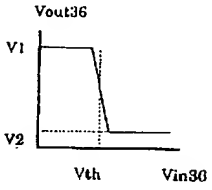

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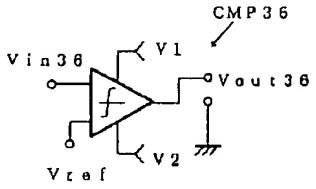

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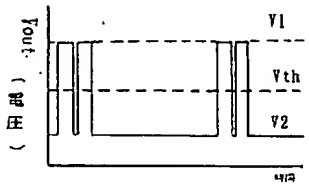

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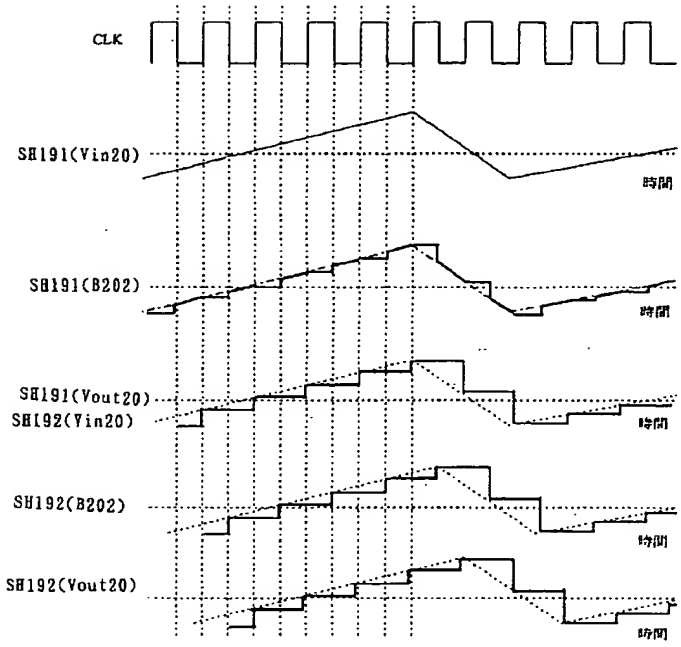

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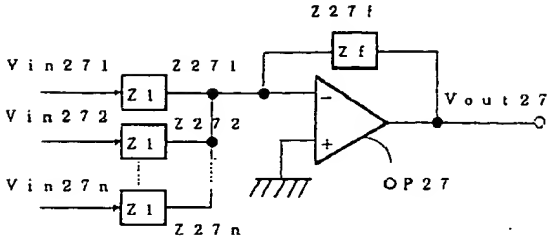

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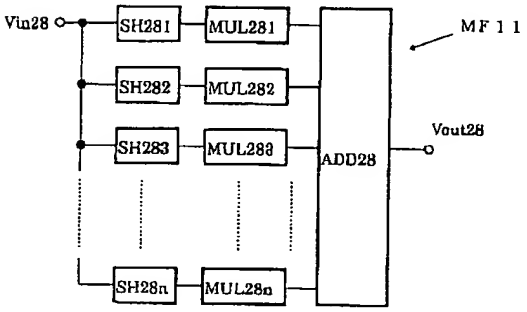

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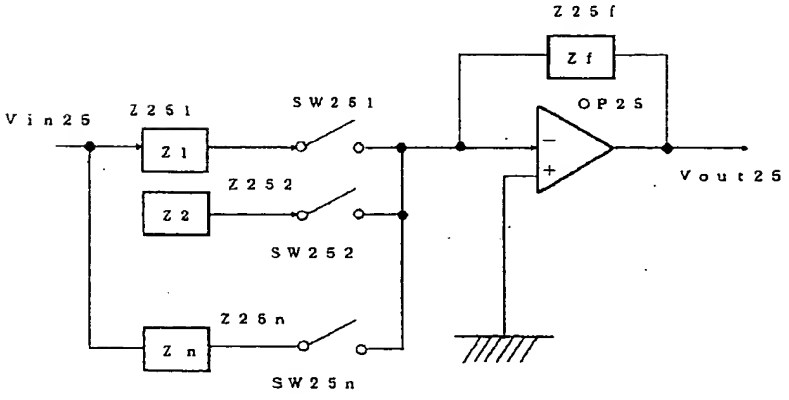

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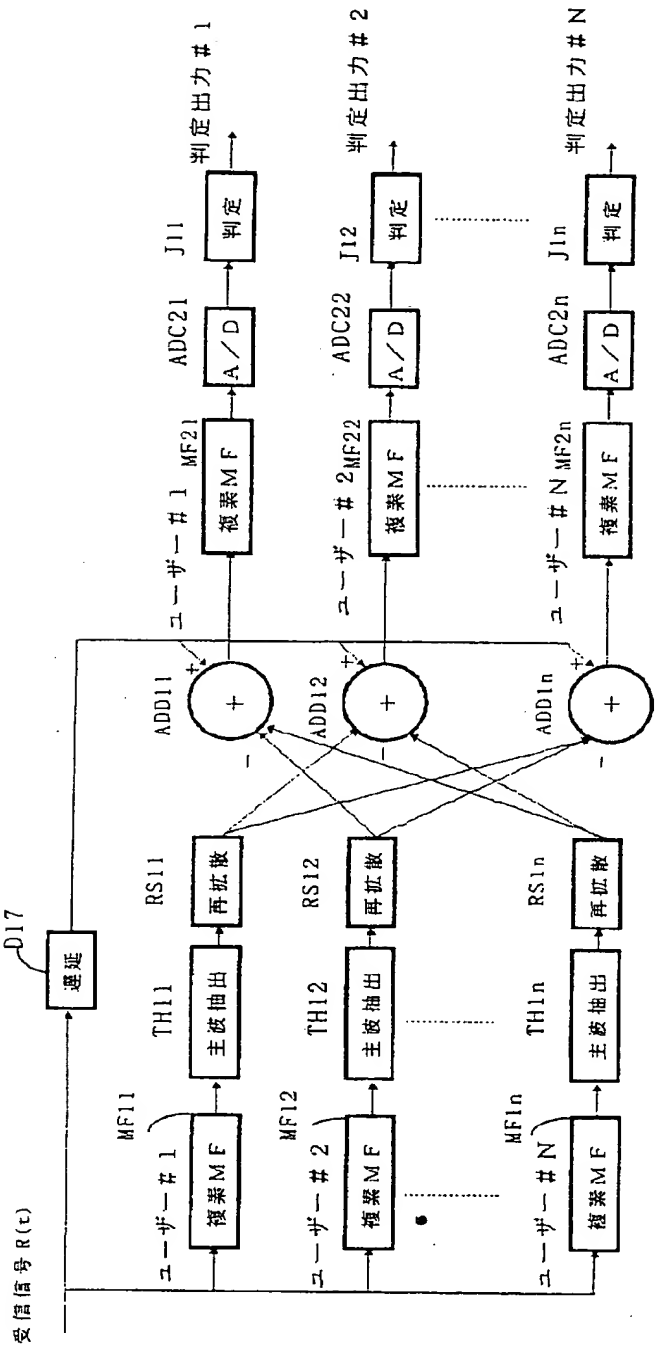
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遅延
ユーザー＃１
ユーザー＃２
ユーザー＃Ｎ
MF11
MF12
MF1n
複素ＭＦ
TH11
TH12
TH1n
主波抽出
RS11
RS12
RS1n
再拡散
ADD11
ADD12
ADD1n
ユーザー＃１
ユーザー＃２
ユーザー＃Ｎ
MF21
MF22
MF2n
複素ＭＦ
ADC21
ADC22
ADC2n
A／D
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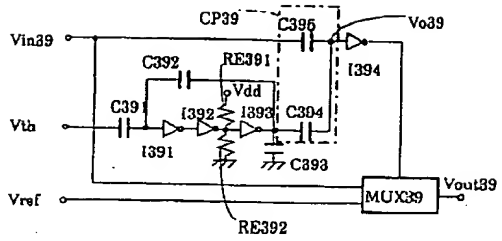
判定出力＃２
判定出力＃Ｎ

【図３９】



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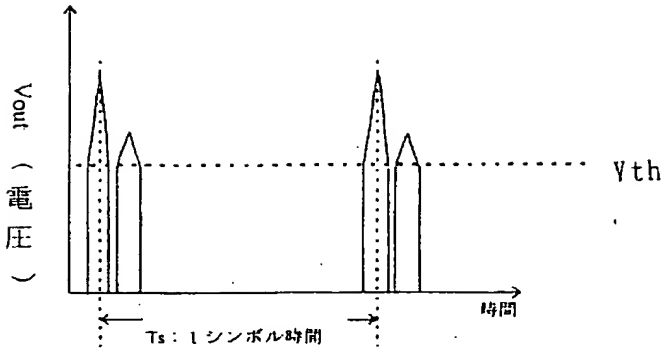

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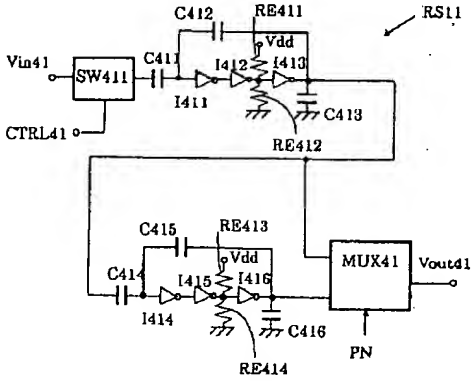

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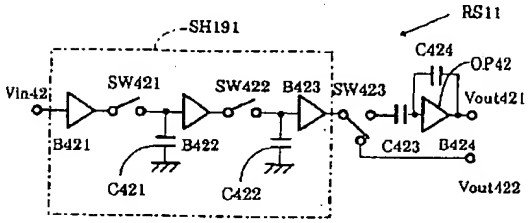

フロントページの続き

(72)発明者　寿　国梁
東京都世田谷区北沢３－５－18　鷹山ビル
株式会社鷹山内

(72)発明者　宮谷　徹彦
東京都中野区東中野三丁目14番20号国際電気株式会社内

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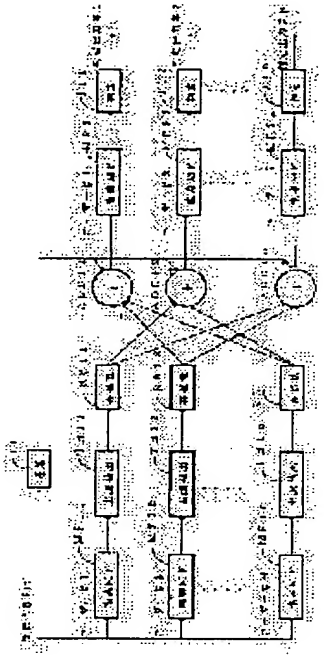
(71)Applicant : KOKUSAI ELECTRIC CO LTD
YOZAN:KK
(72)Inventor : URABE KENZO
SHU NAGAAKI
KOTOBUKI KOKURIYOU
MIYATANI TETSUHIKO

(54) MULTI-USER SIGNAL DEMODULATION METHOD AND DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To solve problems relating to synchronization and to eliminate the need for an interference canceller by applying 2nd spread processing to an extracted signal and reducing a re-spread signal other than a specific user from a received signal so as to extract the received signal.
SOLUTION: Complex matched filters MF11, MF12,...F1n apply inverse spread processing to a reception signal R(t) to extract a signal of each user. Outputs from the matched filters MF11, MF12,...MF1n are given to main wave extract sections TH11, TH12,...TH1n, in which an interference wave and thermal noise are forcibly eliminated. The extracted spread signal component is given to complex matched filters MF21, MF22,...MF2n, in which correlation is calculated and the inverse spread signal component of each user in the received signal is extracted ideally. According to the correlation arithmetic result, discrimination circuits J11, J12,...J1n discriminate the presence of a signal of a corresponding user and provide an output of the signal. The signal extracted in this way is re-spread and a re-spread signal from other users than the specific user is received from the received signal.



LEGAL STATUS

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[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] In case multiplex communication by the DS-CDMA method for N mobile stations (N is the natural number) is performed N the 1st and the 2nd ******** VCFs corresponding to each mobile station are prepared in the receiver of a base station. The diffusion sign assigned to the mobile station corresponding to the 1st and the 2nd ******** VCF is set up as a tap coefficient. every -- Process an input signal with the 1st ******** VCF, carry out threshold processing of the output, and the output more than predetermined level is extracted. An input signal is delayed so that the signal which re-diffused this extracted output with the concerned diffusion sign, and was re-diffused with the above-mentioned input signal may synchronize. the 2nd ******** VCF which subtracts the re-diffusion output of an individual from this delayed input signal (N-1), and has other one diffusion sign of a mobile station -- inputting -- every -- the multiuser recovery technique of judging the signal of each mobile station from the output of the 2nd ******** VCF
[Claim 2] It is the equipment furnished to the receiver of the base station which makes multiplex system the DS-CDMA method whose number of multiuser is N games (N is the natural number). N complex ******** VCFs for an user extraction which perform a correlation acquisition operation while the diffusion sign for the spectrum diffusion assigned to each user is made into a tap coefficient and an input signal is inputted, N principal wave extraction circuits which extract the large incoming wave component (henceforth a principal wave) of power from each user's correlation result obtained from the complex ******** VCF for an user extraction of this N individual, The re-diffusion circuit which performs a spectrum diffusion with the concerned diffusion sign again using the principal wave component obtained from the principal wave extraction circuit of this N individual, The delay circuit from which only the predetermined processing time delays an input signal, and the adder which deducts all outputs other than the concerned user from the output of the above-mentioned delay circuit among the outputs of the N above-mentioned re-diffusion circuits and whose number is N respectively, N complex ******** VCFs for an user recovery which perform a correlation operation again while the diffusion sign for the spectrum diffusion assigned to each user is made into a tap coefficient and the output of the adder of this N individual is inputted, The multiuser demodulator characterized by having N judgment circuits which judge the signal for every user from the output of the complex ******** VCF for an user recovery of this N individual.
[Claim 3] Threshold processing is the multiuser recovery technique according to claim 1 characterized by being set up with the predetermined proportion to the maximum power of the correlation output signal of the 1st ******** VCF.
[Claim 4] A principal wave extraction circuit is a multiuser demodulator according to claim 2 characterized by performing threshold processing by the threshold of predetermined proportion to the maximum power of the correlation output signal of the complex ******** VCF for an user extraction.
[Claim 5] The switch on which a complex ******** filter circuit becomes from two ******** VCFs for I component and each Q component, and each ******** VCF was connected to : (a) input voltage, The 1st capacitance connected to the output of this switch, and the 1st inversion amplifier which consists of an MOS inverter of the odd level connected to the output of this 1st capacitance, The 1st feedback capacitance which connects the output of this 1st inversion amplifier to an input, The 1st multiplexer which outputs alternatively the output or reference voltage of the above-mentioned 1st inversion amplifier, and the output of this 1st multiplexer are two or more sample hold circuits which have the 2nd multiplexer which outputs the 1st-inverting amplifier output or a reference voltage by reverse selection. ;
(b) The 1st addition section which has two or more 2nd capacitance to which the output of the 1st multiplexer of each sample hold circuit was connected, the 2nd inversion amplifier which consists of an MOS inverter of the odd level connected, the output of

these 2nd capacitance being unified, and the 2nd feedback capacitance which connects the output of this 2nd inversion amplifier to an input;
(c) the [the output of the 2nd multiplexer of each sample hold circuit, and] -- the 2nd addition section which has two or more 3rd capacitance to which the output of 1 addition section was connected, the 3rd inversion amplifier which consists of an MOS inverter of the odd level connected, the output of these 3rd capacitance being unified, and the 3rd feedback capacitance which connects the output of this 3rd inversion amplifier to an input, and;
(d) The subtraction section which reduces the output of the 2nd addition section from the output of the above-mentioned 1st addition section;
(e) The claim 1, the 2 written multiuser recovery technique, or equipment characterized by having the control circuit which opens other switches wide and switches the 1st of each sample hold circuit, and the 2nd multiplexer in predetermined combination while the above-mentioned switch in any one in the above-mentioned sample hold circuit is closed, and;.
[Claim 6] A ******** filter circuit is the multiuser recovery technique according to claim 1 or 2 or equipment characterized by having two or more delay circuits into which the input signal was inputted, the multiplication circuit which is connected to the output of each delay circuit and multiplies the concerned output by the PN code, and the adder circuit adding the output of these multiplications circuit.
[Claim 7] It is the multiuser recovery technique according to claim 6 or the equipment which a multiplication circuit is equipped with the operational amplifier by which two or more impedances connected in parallel with an input signal, the switch connected to the output of each impedance, and these switches were connected in parallel with an inversion input, and the noninverting input was grounded, and the feedback impedance which returns the output of this operational amplifier to the above-mentioned inversion input, and is characterized by to close the above-mentioned switch alternatively according to a PN code.
[Claim 8] The switch for signs of 1 input 2 output is connected to the output of an operational amplifier, and the input impedance for signs is connected to the 1st output of this sign switch. The operational amplifier for signs is connected to the output of this input impedance in the inversion input. The output of this operational amplifier for signs is connected to the above-mentioned inversion input through the feedback impedance for signs. The feedback impedance for signs is set up equally to the input impedance for signs. It is the multiuser recovery technique according to claim 7 or equipment characterized by the switch for signs being connected to the 1st output, and the output of the operational amplifier for signs being made into a multiplication result when a PN code is positive, and making the 2nd output of the switch for signs into a multiplication result when a PN code is negative.
[Claim 9] They are the multiuser recovery technique according to claim 6 of carrying out an adder circuit being equipped with the operational amplifier for an addition by which the output of the input impedance for an addition to which the output of each multiplication circuit was connected, and the input impedance for these additions was connected in parallel with an inversion input, and the noninverting input was grounded, and the feedback impedance for an addition which connects the output of this operational amplifier for an addition to the above-mentioned inversion input, and the feedback impedance for an addition being set up equally to the input impedance for an addition as the
[Claim 10] A delay circuit is a multiuser demodulator according to claim 2 or 6 which connects two or more sample hold circuits to a serial from the first rank to the last card row, inputs an input signal from this first rank, and is transmitted to the last card row one by one.
[Claim 11] A sample hold circuit is a multiuser demodulator according to claim 10 characterized by connecting the switch for a buffer circuit and sample hold in series by turns, and having connected grounding capacitance to the output of each switch.
[Claim 12] A buffer is a multiuser demodulator according to claim 11 which a noninverting input is considered as an input and characterized by an output consisting of an operational amplifier which returned to the inversion input.
[Claim 13] A buffer is a multiuser demodulator according to claim 11 characterized by consisting of an operational amplifier by which the output of the impedance for an input and this impedance for an input was connected to the inversion input, and the noninverting input was grounded, and an impedance for feedback which it is set impedance] up equally to the above-mentioned impedance for an input, and returns the output of the operational amplifier of a parenthesis to the above-mentioned inversion input.
[Claim 14] A principal wave extraction circuit is a multiuser demodulator according to claim 2 characterized by being the operational amplifier as which the input signal was

inputted into the noninverting input, and the threshold voltage was inputted into the inversion input.
[Claim 15] It is the multiuser demodulator according to claim 2 which a principal wave extraction circuit is equipped with capacity coupling adding the multiplexer which outputs an input signal and a reference voltage alternatively, and inversion and the input signal of a threshold voltage, and is characterized by switching and controlling the above-mentioned multiplexer according to this addition result.
[Claim 16] the [the 1st inversion buffer with which a re-diffusion circuit inverts the output of the switch to which input voltage was connected, and this switch, the 2nd inversion buffer which inverts the output of this 1st inversion buffer, the 1st inversion buffer, or] — the multiuser recovery technique [equipped with the multiplexer which outputs any of 2 inversion buffer, or one output alternatively] according to claim 1 or 2, or equipment
[Claim 17] A re-diffusion circuit is the multiuser recovery technique according to claim 1 or 2 or equipment equipped with the sample hold circuit to which input voltage was connected, and the inversion buffer by which the output of this sample hold circuit was connected to the 1st output of the switch of 1 input 2 output, and this switch.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to the multiuser demodulator for the receiver of a base station in a spectrum diffusion communication of a DS-CDMA (Direct Sequence-Code Division Multiple Access) method.
[0002]
[Description of the Prior Art] Although the separation extraction of each user's signal needed to be carried out and back-diffusion of gas of the extracted signal needed to be carried out in the base station receiver of a DS-CDMA method spectrum diffusion communication, having received the signal from two or more users, and taking an interference etc. into consideration, the correlation operation for back-diffusion of gas was performed in many cases using slide ********** (it is called below Sliding Correlator:SC) which consists of a former comparatively simple circuit. And it was required that the phase simulation of the diffusion sign of an input signal and the diffusion sign of a receiver was perfect, and synchronous usurpation and holding circuits, such as DLL (DelayLocked Loop), were required for SC. However, since it was difficult for DLL to have the fault that initial drawing-in time and re-drawing-in time are size, and to realize a perfect synchronization generally, the degradation of the receiving property by the imperfection of a synchronization arose.
[0003] Although the interference canceller was conventionally used in order to prevent the interference between each user's signals furthermore After this interference canceller passes through processing of the back-diffusion of gas of an input signal, rake synthesis, etc. Although the input signal for a specific user was extracted by reproducing the input signal corresponding to each user's signal, and reducing the reproduction signal of users other than a specific user from an input signal by spectrum diffusion, the circuit was very large-scale and expensive.
[0004]
[Problem(s) to be Solved by the Invention] It aims at having been originated that such a conventional trouble should be canceled, and this invention canceling the trouble relevant to the synchronization, and an interference canceller offering the unnecessary multiuser recovery technique and unnecessary equipment.
[0005]
[Means for Solving the Problem] The multiuser recovery technique concerning this invention extracts a specific user's signal by only carrying out threshold processing of the signal which carried out back-diffusion of gas of the input signal, re-diffuses the extracted signal and extracts the input signal for a specific user by reducing re-diffusion signals other than a specific user from an input signal.
[0006]
[Embodiments of the Invention] Next, one example of the multiuser recovery technique concerning this invention is explained based on a drawing.
[0007]
[Example] Drawing 1 shows notionally one example of the multiuser recovery technique concerning this invention, carries out back-diffusion of gas of the input-signal R (t) in complex ******** VCFs MF11 and MF12, ..., MF1n, and extracts each user's signal. Each user's signal extracted here has received asymmetry by the transmission line, and thermal noise is further included in the input signal. When ai and each user's diffusion sign are set to PNi and thermal noise is set [the signal of each user who took transmission-line asymmetry into consideration here] to n (t) for Ii (t) and its receiving level, input-signal R (t) is [Equation 1].

$$R(t) = a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \cdots + an \cdot PNn \cdot In(t) + n(t) \qquad (1)$$

It is expressed.
[0008] For example, if input-signal R (t) is processed by 1st ******** VCF MF11, the output voltage of the solid line of drawing 2 arises, and two or more peaks P1, P2, and

P3 have appeared in this output voltage at every one period (1 symbol time). The voltage shown as a solid line is the correlation result of an operation of the 1st term of a formula (1) and a thermal-noise term, and the 1st-user diffusion sign. Moreover, an alternate long and short dash line is an interference-wave voltage, and is the correlation result of an operation of the sum of the 2nd term of a formula (1), - the n-th term, and the 1st-user diffusion sign.

[0009] Generally, although the diffusion sign given to each user has a high orthogonality, and the level of an interference wave is low since a cross-correlation is low, if the number of users increases, the level of an interference wave will become high as shown in drawing 2 , and an exact peak detection will become difficult in a DS-CDMA method.

[0010] Then, the output of ******** VCF MF11 - MF1n is inputted into the principal wave extraction sections TH11 and TH12, ..., TH1n, and removes an interference wave and thermal noise compulsorily. It is processing which a principal wave extraction is processing] threshold processing, and the inside P3 of the peaks P1-P3 in drawing 2 is notionally eliminated [processing] as a peak below predetermined level here, and produces a wave as shown in drawing 3 . However, in actual threshold processing, since the input below a threshold is changed into the signal of a low, the output of the drawing 38 or the drawing 40 produces it in fact. The principal wave extraction section makes a threshold the voltage which applied predetermined proportion to the peak voltage which gives the maximum power within 1 symbol time, and carries out threshold processing of the input signal. The output of the principal wave extraction section is inputted into the re-diffusion sections RS11 and RS12, ..., RS1n, respectively, and a spread spectrum is performed again. This re-diffusion output is the replica signal approximated to the input signal for each user, for example, the output of RS11 is a replica signal for users other than the 1st.

[0011] The diffusion signal for each user is generated using the above replica signal. That is, in generation of the diffusion signal for the i-th user, the sum of the replica signal of users other than the i-th is subtracted from input-signal R (t) in adder ADD1i. Input-signal R (t) is delayed by the delay circuit D1, and the timing with the processing result by the ******** VCF, the principal wave extraction section, and the re-diffusion circuit is adjusted. Supposing the status with an ideal replica signal, i.e., the i-th term of a formula (1), is extracted, an adder output will serve as the diffusion signal component for the i-th user, and the sum of thermal noise, as shown in a formula (2).

[Equation 2]

$$\begin{aligned} Aouti &= R(t) - \{a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \ldots + ai-1 \cdot PNi-1 \cdot Ii-1(t)\} \\ &\quad - \{ai+1 \cdot PNi+1 \cdot Ii+1(t) + \ldots + an \cdot PNn \cdot In(t)\} \\ &= ai \cdot PNi \cdot Ii(t) + n(t) \end{aligned} \qquad (2)$$

In the output of an adder, it turns out that the influence of a cross-correlation, i.e., an interference, can be mitigated so that clearly from a formula (2).

[0012] Thus, the correlation operation of the extracted diffusion signal component is carried out by complex ******** VCFs MF21 and MF22, ..., MF2n, and, ideally, the back-diffusion-of-gas signal component of each user in an input signal is extracted. In the judgment circuits J11 and J12, ..., J1n, presence of a correspondence user's signal is judged to this correlation result of an operation, and the signal is outputted.

[0013] Here, the effect of the example of drawing 1 is shown through various ******** VCF outputs when the multi-pass has not arisen.

[0014] Drawing 4 shows the example of a simulation of the output of above-mentioned ******** VCF MF21 when there are very few interferences. The conditions of a simulation are made into primary modulation QPSK, a diffusion sign 128 chip M sequence, the exaggerated measurement size 4, and two user numbers here, and it is a correlation operation under the static conditions in a baseband band. In this drawing, the 1st user's (it considers as the office of choice.) correlation peak is detected at the time of t= 0. Moreover, 100dB and the wave motion power pair interference-wave power ratio (D/U) of choice of the signal energy pair noise power flux density per bit (Eb/No) are 100dB, and the influence of a noise and an interference performed parvus conditioning extremely. In addition, the peak in time t= 512 is unrelated to the impulse response of a transmission line according to the contiguity symbol.

[0015] Drawing 5 is what carried out 16 symbol time display of the ******** VCF output of drawing 4 , and shows simultaneously the real-number component (I phase) and the imaginary number component (Q phase). Therefore, when there is only one peak, I phase and Q phase have the same polarity, and that a peak exists up and down shows that I phase and Q phase are an antiphase mutually. As shown in drawing, on such ideal conditions, a clear peak arises and the interference by other users is not produced.

[0016] Drawing 6 is as a result of [which ten interference offices other than D/U=-10dB, i.e., the office of choice, exist, and shows the status of =(wave motion power of choice)0.1x (interference-wave power)] a simulation. Here, the big interference peak other than the office peak of choice of t= 0 is produced at the time of t= 270. It is generated when it differs if a diffusion sign changes, since it is influenced by the cross-correlation value, and this interference peak causes an incorrect judging. Or the office peak level of choice may decline by presence of an interference peak, and it is easy to produce an incorrect judging also at this point.
[0017] Drawing 7 is a ******** VCF output for interference offices in the same conditions as drawing 6 , and the interference office peak has produced it more clearly than the office peak of choice of drawing 6 . Although it is the position of this peak at the time of t= 128, it is based on this having adopted the method of asynchronous CDMA. With asynchronous CDMA, each user's diffusion sign is made asynchronous into the same cell here. The diffusion sign phase of an interference wave is shifted as the worst conditions this time by 128 samples which become the worst [a cross-correlation value] (a part for 32 chips).
[0018] Drawing 8 carries out 16 symbol term display of the ******** VCF output of drawing 6 . In this case, the office peak of choice which should be produced in t= 0 is unstable, and the detection is impossible. That is, it also understands a certain thing that the office of choice is buried with some level of a cross-correlation value.
[0019] In the comparison with the above graph, the result which removed the interference wave according to the example of drawing 1 is shown in drawing 9 . That is, drawing 9 shows the result which removed the interference wave according to the example of drawing 1 , the peak of the office of choice is stabilized, and the almost same property as the case (drawing 5) where an interference wave does not exist is acquired. That is, elimination of an interference wave can detect the office peak of choice now certainly.
[0020] Next, the case where a multi-pass arises is explained.
[0021] Drawing 10 is a ******** VCF output when carrying out 3 pass static conditions of the impulse response of a transmission line, the direct wave of the office of choice arises in t= 128, and the retardation wave motion has produced it in t= 138 and t= 148. here -- the gain of each pass -- 1.0 and 0. -- it is set as 7 and 0.5
[0022] drawing 11 -- the multi-pass signal of drawing 10 -- Eb/No=100dB (there is almost no influence of a noise.), and D/U=-10dB (the influence of an interference wave is large.) -- the ******** VCF output of 16 symbol time is displayed on the bottom of conditions in this drawing, since interference-wave level is high, the peak of the office of choice can be recognized -- it has become
[0023] Drawing 12 performs interference cancel by the example of drawing 1 to the same multi-pass signal as drawing 11 , and the direct wave of the office of choice serves as a clear peak, it appears, and it turns out that it can perform a peak detection certainly.
[0024] Drawing 13 is a graph which shows the bit error rate to Eb/N0 variously, and compares the bit error rate (a dashed line and a balloon plot show.) by the example of drawing 1 , the bit error rate (dashed line) when not performing interference-wave cancel at all, and a bit error rate theoretical value (solid line). When not performing interference-wave cancel from drawing, as compared with this example, a bit error rate increases several 10 times from several times, and this example serves as the value approximated to the theoretical value.
[0025] Processing of complex ******** VCF MF11 in the example of drawing 1 - MF1n, MF21-MF2n, the principal wave extraction section TH11 - TH1n, re-diffusion section RS11 - RS1n, adder ADD11 - ADD1n, and the judgment circuit J11 - J1n is realizable with various modes so that it may illustrate below.
** The mode which realized the whole by software on the general purpose computer.
** For CPU, it is the mode which realized only the ******** VCF with a high calculation load by DSP or the digital circuit of exclusive use, and realized other fractions by software.
** The mode which realized the whole by DSP or the digital circuit of exclusive use.
** For CPU, it is the mode which realized only the ******** VCF with a high calculation load by the analog circuit, and realized other fractions by software.
** The mode which realized only the ******** VCF by the analog circuit and realized other fractions by DSP or the digital circuit of exclusive use.
** The mode which realized the whole by the analog circuit.
In order to raise processing speed, it is necessary to raise the proportion of an analog or a digital personal circuit and, and in these modes, the analog circuit is more advantageous than the digital circuit in respect of power consumption.
[0026] Drawing 14 shows ******** VCF MF11 by the exclusive digital circuit, and drawing 15 shows the principal wave extraction section TH11 by the exclusive digital circuit.

[0027] In drawing 14 , ******** VCF MF11 has shift register SFTREG of n stage where the digitized input signal Vin14 is inputted, and the multiplication circuit MUL141 - MUL14n are connected to each stage of a shift register, respectively. The PN code is set to each multiplication circuit as a multiplier, and the operation which multiplies by the PN code to an input signal is performed. And all the outputs of a multiplication circuit are inputted into adder-circuit ADD14, and are integrated in here. The addition result Vout14 is the so-called ******** VCF output. In addition, since a PN code is usually 1-bit data, the AND gate which passes each bit of an input signal is sufficient for a multiplication circuit.
[0028] The principal wave extraction circuit TH11 has shift register SFTREG which holds the ******** VCF output Vin15 by 1 symbol time, and comparator circuits C1-Cn are connected to each stage of this shift register. the first rank of a shift register -- a stage is connected to the maximum circuit MAX and the feedback data from the latter multiplexer MUX are inputted into this maximum circuit The output of the maximum circuit MAX is connected to registers REG1 or REG2 through a selector SEL, and a multiplexer MUX outputs the output of these registers alternatively. the data with which the maximum circuit was outputted from MUX, and the new first rank -- stage data are compared and larger data are inputted into a new register When the data outputted here from MUX are a thing from REG1, REG2 serves as a new register and serves as the register with new REG1 to REG2. Therefore, large data will be registered into REG1 and REG2 by alternation. A selector is switched to a register always new and a multiplexer is switched in response to this.
[0029] The output of a multiplexer is further connected to the multiplication circuit MUL, and the threshold Vth which applied predetermined proportion to maximum here is computed. The threshold computed here is inputted into comparator circuits C1-Cn, and is compared with the data of each stage of a shift register. The comparison result is as being shown in drawing 16 , only the data more than Vth are outputted as it is, and the data of under Vth are omitted by 0V. Processing of the above-mentioned principal wave extraction is attained by this.
[0030] Drawing 17 shows one example of the demodulator concerning this invention, realizes the principal wave extraction section, the re-diffusion section, and a judgment circuit by the exclusive digital circuit, and has realized others by the exclusive analog circuit.
[0031] In drawing 17 , input-signal R (t) is inputted into ******** VCF MF11 - MF1n, and the delay circuit D17 of an analog, and the output of MF11 - MF1n passes through A/D-conversion circuit ADC11 - ADC1n, and is inputted into the digital principal wave extraction circuit TH11 - TH1n, and re-diffusion circuit RS11 - RS1n. The output of RS11 - RS1n is inputted into adder-circuit ADD11 - ADD1n through D/A-conversion circuit DAC11 - DAC1n, and is subtracted from the output of a delay circuit D17. The output of an adder circuit is inputted into ******** VCF MF21 - MF2n, and is again inputted into the judgment circuit J11 - J1n through A/D-conversion circuit ADC21 - ADC2n after that.

[0032] drawing 18 -- setting -- the analog delay circuits D181 and D182 of a plurality [MF / ******** VCF /11 / of an analog], ..., D18n -- in-series -- connecting -- input-signal R (t) of an analog -- the first rank -- it is transmitted to the latter part one by one from a delay circuit, and results in last card row delay circuit D18n The analog multiplication circuit MUL181, ..., MUL18n are connected to the output of each delay circuit, and PN codes PN1, PN2, ..., PNn are hung on an input signal in these multiplications circuit. The output of the multiplication circuit MUL181 - MUL18n is inputted into adder-circuit ADD181, and all multiplication results are added. If delay time in the delay circuit D181 - D18n is set to Tc, the following operations will be performed with the above ******** VCF.
[Equation 3]

$$S(t) = \sum_{i=1}^{n} PNi \cdot R(t - i \cdot Tc) \qquad (3)$$

In addition, the above configuration is the same also about MF12 - MF1n, and MF21-MF2n.

[0033] drawing 19 -- setting -- the sample hold circuit SH191 of a plurality [delay circuit / D17], - SH19n -- in-series -- connecting -- the first rank -- the input voltage Vin19 inputted into the sample hold circuit SH191 is transmitted to the latter part one by one, and each sample hold circuit performs sample hold of data in response to a clock CLK19 The number of stages of a delay circuit and the timing of a clock are set up so that it may synchronize with the timing to which input-signal R (t) arrives at an adder circuit through a ******** VCF, the principal wave extraction section, and the re-diffusion section. In addition, it is also possible for a delay circuit to have the function of a shift register and to use the output Vout191 from each sample hold

circuit - Vout19n as data as it is. In addition, the analog delay circuit in drawing 18 also becomes the same configuration as drawing 19 .
[0034] A sample hold circuit SH191 is constituted as shown in drawing 20 , it connects a buffer B201, the switch SW201, the buffer B202, the switch SW202, and the buffer B203 to a serial one by one, and comes to connect the grounding capacitance C201 and C202 with the latter part of switches SW201 and SW202. Input voltage Vin20 is inputted into a buffer B201, and a buffer outputs Vin20 stably irrespective of a latter load. When SW201 is closed, the charge and discharge of the grounding capacitance C201 will be carried out to the charge corresponding to the output voltage of a buffer B201, and a voltage will be held with capacitance C201. After the completion of a hold, a switch SW201 is opened wide and a hold of the following input voltage is equipped with it. The held voltage turns into the input voltage of a buffer B202, and is stably outputted from a buffer B202. If a switch SW202 is closed here, according to the output voltage of a buffer B202, the charge and discharge of the grounding capacitance C202 will be carried out, and the output of a buffer B202 will be held. The voltage held with the grounding capacitance C202 turns into the input voltage of a buffer B203, and is outputted to the latter part as a stable output Vout20 of a buffer B203.
[0035] Switches SW201 and SW202 are closed by turns to predetermined timing, and input voltage Vin20 is transmitted and held one by one C201 and C202. And since the voltage transmitted to C202 is not influenced of input voltage Vin20 to closing of the next switch SW202, it can generate the stable output Vout20.
[0036] As a buffer B201, a ********** follower type (drawing 21) or an inversion buffer type (drawing 22) can be adopted.
[0037] A buffer B201 connects input voltage Vin21 to the noninverting input of an operational amplifier OP21, and makes output voltage Vout21 come to return to the inversion input in drawing 21 . In this circuit, the ratio of I/O is set to +1 and an input arises in an output as it is.
[0038] The circuit of drawing 22 grounds the noninverting input of an operational amplifier OP22, and comes to connect input voltage Vin22 with an inversion input through an impedance Z221. Moreover, the output of an operational amplifier OP22 has returned to the inversion input through the impedance Z221 and the equal impedance Z222. The output Vout22 of this circuit is equal to -Vin22, and since input voltage is outputted in a sample hold circuit through three steps of buffers B201, B202, and B203, the final output is inverted. Therefore, although the final output Vout19 (drawing 19) serves as the same sign as Vin19 when the sample hold circuit in a delay circuit is even level, at the time of odd level, you should add the buffer for reversing an input or an output further. In addition, since the sample hold circuit SH192 - SH19n are constituted like SH191, they omits an explanation.
[0039] Drawing 23 is a graph which shows an operation of a sample hold circuit, and shows input voltage (Vin20), the 2nd step buffer (B202) output, and output voltage (Vout20) in the relation with a clock CLK20 about SH191 and SH192.
[0040] If a switch SW201 is closed in Vin20 to SH191 changing now (CLK20 is a low), Vin20 will appear as B202 output of SH191 as it is during the closed period. B202 output is fixed until B202 output is held and CLK20 is again set to a low, when SW201 is opened (CLK20 is a high level). A switch SW202 is closed at the time of the high level of CLK20, generates the voltage which held the voltage held at the time of SW201 opening one by one by one period of CLK20, and outputs it as Vout20.
[0041] The output of a sample hold circuit SH191 serves as the input voltage (Vin20) of the 2nd step of sample hold circuit SH192, is held in SH192 to the timing for which CLK20 was delayed by the half period in input voltage by SW201, generates the voltage which carried out the half-period retardation of it further by SW202, and outputs it as output voltage Vout20.
[0042] As compared with a digital type delay circuit, a circuit scale is small, and the delay circuit above analog type has slight power consumption.
[0043] Drawing 24 shows the 2nd example of a sample hold circuit. This sample hold circuit realizes the same property as an inversion buffer by three steps of CMOS inverters I241, I242, and I243, the output of I243 returns to the input of I241 through the feedback capacitance C242, and input voltage Vin24 is connected to the input of I241 through the CMOS switch SW241 and the input capacitance C241 one by one.
[0044] If it is wide opened once SW241 is closed, the charge and discharge of C241 will be carried out to the charge according to Vin24 at the time. C242 is set up equally to C241, and the three step inverters I241-I243 output the voltage held by C241 as an output of I243 as it is. The CMOS switch SW242 is connected to the output of I243, and the hold of input voltage and the output are possible by opening and closing SW241 and SW242 by turns like the sample hold circuit of drawing 20 .
[0045] Furthermore, an output is inputted into SW242 through capacitance C244 at the same three step CMOS inverters I244, I245, and I246 as the above, and the output of

I246 is connected to the input of I244 through the feedback capacitance C245. The sign of I/O of a sample hold circuit has consistency by this.
[0046] The grounding capacitance C243 and C246 as a low pass filter is connected to the output of a last card row MOS inverter, and, as for these three steps inverter, one pair of balanced resistances RE241, RE242, RE243, and RE244 are connected to the 2nd step of output. RE241 and RE243 are connected to supply voltage Vdd, and RE242 and RE244 are grounded and have suppressed the gain of a three step inverter. By such circuit arrangement, the oscillation of the three step inverter containing the feedback system is prevented.
[0047] Drawing 25 shows the multiplication circuit of above-mentioned ******** VCF MF11, leads input voltage Vin25 to the impedances Z251 and Z252 from which a plurality is different, ..., Z25n, and has inputted the output of these impedances into the inversion input of an operational amplifier OP25 in arbitrary combination by the switch SW251 - SW25n. A noninverting input is grounded and, as for the operational amplifier OP25, the output has returned to the inversion input through feedback-impedance Z25f. An operational amplifier OP25 constitutes an inversion buffer, and each impedance consists of a capacitor. Impedance Z25i is [Equation 4] by capacitor C25i here.

$$Z25i = \frac{1}{j\omega C25i} \qquad (4)$$

When the sum of the capacity of the capacitor by which it was expressed and the switch was closed is expressed as sigmaC25i, output voltage Vout25 is [Equation 5].

$$Vout25 = -\frac{\sum C25i}{C25f} Vin25 \qquad (5)$$

It becomes. This means the multiplication which multiplied by - (C25i/C25f) to Vin25. If SW251 - SW25n are closed in arbitrary combination, for example, the capacity of C25i is set as the exponentiation of 2, the multiplication of the arbitrary multipliers of a binary digit will become possible. in addition, a PN code -- as for such a weighting, or (1, 0) (1, -1) is unnecessary at the time of binary
[0048] In addition, as shown in a formula (5), since it is reversed, when using this as an output as it is, the inversion buffer which reverses a sign further is required for the sign of an output. Moreover, the sign of a coefficient is not contained in the formula (5). Drawing 26 is an addition circuit for this inversion or sign adjustment, and according to the sign of a multiplier (PN code), Vout25 is led to an inversion buffer, or it carries out a direct output. An inversion buffer grounds a noninverting input while it connects an impedance Z26 to the inversion input of an operational amplifier OP26, and it is returning the output of OP26 to the inversion input. The output Vout261 which went via the inversion buffer corresponds to a positive PN code, and a direct output Vout262 corresponds to a negative PN code.
[0049] Drawing 27 shows adder-circuit ADD181 kicked to ******** VCF MF11. Adder-circuit ADD181 grounds a noninverting input, and is returning the output of an operational amplifier OP27 to the inversion input through impedance Z27f further while it connects the impedance Z271 - Z27n in parallel with the inversion input of an operational amplifier OP27. It is [Equation 6], when an impedance consists of capacitor C27i - C27n and C27f, and the input to each impedance is set to Vin271 - Vin27n and it sets an output to Vout27.

$$Vout27 = -\frac{\sum_{i=1}^{n} Vin27iC27i}{C27f} \qquad (6)$$

[0050] Drawing 28 shows ******** VCF MF11 for the binary PN code of (1, 0), ******** filter circuit MF11 has the sample hold circuit SH281 of a plurality (n pieces), - SH28n, and the parallel input of the input signal Vin28 is carried out at these sample hold circuits.
[0051] A sample hold circuit SH281 is constituted as shown in drawing 29 , and input voltage Vin29 is connected to the switch SW29. The output of a switch SW29 is connected to capacitance C291, and three steps of in-series MOS inverters I291, I292, and I293 are connected to the output of capacitance C291. It connects with the input of I291 through the feedback capacitance C292, and Vin29 produces the output Vo29 of the MOS inverter I293 of the last card row in the output of I293 with a good linearity by this. If SW29 is closed, C291 will be charged by the charge corresponding to Vin29, and the alignment property of an output will be guaranteed by the feedback function of I291-I293. And when a switch SW29 is opened wide after that, a sample hold circuit SH281 will hold Vin29. The output of I293 of the last card row is connected to a gland

through the grounding capacitance C293, and the 2nd-step output of I292 is connected to the supply voltage Vdd and the gland through one pair of balanced resistances R291 and RE292. By such configuration, the oscillation of the inversion amplifying circuit containing the feedback system is prevented. In addition, since the sample hold circuit SH282 - SH28n are constituted like SH281, they omits an explanation.

[0052] As shown in drawing 30 , the above-mentioned multiplication circuit MUL11 consists of two multiplexers MUX301 and MUX302, and the above Vo29 and the common reference voltage Vr are connected to these multiplexers.

[0053] Switch SW and the multiplexers MUX301 and MUX302 are controlled by the control signals S1, S2, and S3, and once closing S1, when it should incorporate input voltage, it opens SW29. S2 and S3 are the inverted signals, and when one multiplexer outputs Vo29, the multiplexer of another side outputs Vr. MUX301 and MUX302 output Vo29 from MUX301, when it corresponds to "1" (high level) of a diffusion sign, and "-1" (low) and the input voltage at a certain time should be multiplied by the sign "1", and when it should multiply by "-1", they output Vo29 from MUX302. Since this highness and the level of a row are represented, in drawing 30 , VH and the output of MUX302 are displayed for the output of MUX301 by VL.

[0054] As shown in drawing 31 , a switch SW29 consists of a transistor circuit T31 which connects the source of n type MOS transistor, and a drain with the drain of p type MOS transistor, and the source, respectively, and becomes, connects input voltage Vin31 to the terminal by the side of the drain of nMOS of this transistor circuit, and comes to connect the terminal of the source of nMOS with an output terminal Vout31 through the dummy transistor DT31 of the same configuration. S1 is inputted into the gate of nMOS transistor in a transistor circuit T31, and the signal which inverted S1 by the inverter I31 is inputted into the gate of pMOS transistor. When S1 is high-level, T31 flows, and T31 is intercepted by this when it is a low.

[0055] As shown in drawing 32 , the drain of one pair of MOS transistors of n type and p type [multiplexer / MUX301], In the terminal by the side of the drain of nMOS [in / it comes to connect with the common output terminal Vout32 the terminal by the side of the source of nMOS of the transistor circuits T321 and T322 which come to connect the source mutually, and / T321], it is the output Vo29 (it is shown all over [Vin321] drawing.) of the MOS inverter I293. It connects and is a reference voltage Vr (it is shown all over [Vin322] drawing.) in the drain of T322. It connects. A signal S2 is inputted into the gate of nMOS transistor in a transistor circuit T321, and the gate of pMOS transistor in a transistor circuit T322, and the signal which inverted S2 by the inverter I32 is inputted into the gate of nMOS of pMOS and T322 of T321. When S2 is high-level, T321 flows, T322 is intercepted by this, T322 flows at the time of a low, and T321 is intercepted. That is, MUX301 may output Vo29 or Vr alternatively with control of S2.

[0056] Although illustration is omitted, a multiplexer MUX302 is constituted like MUX301, and connection of Vo29 and Vr has reversed it. That is, it is the configuration of having connected Vr to T321 and having connected Vo3 to T322. By this, MUX302 outputs Vo29, when the output 301 opposite to MUX301, i.e., MUX, outputs Vo29 and MUX301 outputs Vr for Vr.

[0057] A signal S2 corresponds to a diffusion sign, and when S2 is "1", the multiplication circuit MUL11 outputs Vr and MUX302 to Vo29 from MUX301, when S2 is "0" about Vo29 and MUX302 to Vr from MUX301. These outputs are led to above-mentioned adder-circuit ADD28. That is, although the signal of one line from MUL281 to ADD28 is described, this represents two signals, a high-level side and a low side, with drawing 28 .

[0058] In drawing 33 , adder-circuit ADD28 has the capacity coupling CPL as which the low signals VL1-VLn from the capacity coupling CPH and MUL281 - MUL28n into which the high-level signals VH1-VHn from MUL281, MUL282, ..., MUL28n were inputted were inputted, CPL comes to carry out parallel connection of the capacitance CL1-CLn, and CPH comes to carry out parallel connection of the capacitance CH1-CHn. the first rank of the MOS inverters I331, I332, and I333 with the output of CPL in-series three steps -- it connects with an input -- having -- the output of I333 -- the feedback capacitance C331 -- minding -- the first rank -- it is fed back to the input This three step inverter has guaranteed the linearity of input/output relation according to sufficient big its open loop and gain.

[0059] the first rank of the MOS inverters I334, I335, and I336 with the output of CPH in-series three steps -- it connects with an input -- having -- the output of I336 -- the feedback capacitance C333 -- minding -- the first rank -- it is fed back to the input This three step inverter has guaranteed the linearity of input/output relation according to sufficient big its open loop and gain. Furthermore, the output of I333 is connected to the input of I334 through joint capacitance CC33 in parallel with capacity coupling CPH, and the sum of inversion of the output of CPL and the output of CPH is

inputted into the three step inverters I334-I336.
[0060] The output of the MOS inverters I333 and I336 of the last card row in the above-mentioned three step inverter is connected to a gland respectively through the grounding capacitance C332 and C334, and the output of the 2nd step of MOS inverters I332 and I335 is connected to the supply voltage Vdd and the gland respectively through one pair of balanced resistances R331, R332, R333, and R334. By such configuration, the oscillation of the inversion amplifying circuit containing the feedback system is prevented.
[0061] Adder-circuit ADD28 performs the operation of a formula (7), and since the relation between capacitance is set up like formula (8) - (10), the formula (11) result of an operation is obtained as a result.
[Equation 7]

$$Vout33 = Vdd - \frac{\left(Vdd - \frac{\sum_{i=1}^{n} VLi \cdot CLi}{C331} \right) \cdot CC33 + \sum_{i=1}^{n} VHi \cdot CHi}{C333} \quad (7)$$

$$CL1 = CL2 = \ldots = CLn \quad (8)$$

$$CH1 = CH2 = \ldots = CHn \quad (9)$$

$$C331 = C333 = CC33 = n \cdot CLi = n \cdot CHi \quad (10)$$

$$Vout33 = \frac{\sum_{i=1}^{n} (VLi - VHi)}{n} \quad (11)$$

[0062] VLi and Vhi are changed into representation of the formula (12) on the basis of a reference voltage Vr, and (13) here.
[Equation 8]

$$VHi = Vr + vhi \quad (12)$$

$$VLi = Vr + vli \quad (13)$$

A formula (14) will be obtained if this formula (12) and (13) are substituted for a formula (11).
[Equation 9]

$$Vout33 = \frac{\sum_{i=1}^{n} (vli - vhi)}{n} \quad (14)$$

[0063] Furthermore, a formula (14) is rewritten by the formula (15), when the signal which held the input signal Vin1 to time series by the sample hold circuit SH31 - SH3n when a certain time was set to t and chip time was set to Tc and natural number i sets to Pni S (t-i and Tc) and the PN code by which this is multiplied, since inversion of the data by the three step inverter is performed also in the sample hold circuit.
[Equation 10]

$$Vout33 = \frac{\sum_{i=1}^{n} PNi \cdot S(t - i \cdot Tc)}{n} \quad (15)$$

This is the operation of a common ******** VCF.
[0064] In addition, since the output is normalized by number n of an input in the above operation, it is prevented that the maximum voltage of an output exceeds supply voltage, and the stability of operation is guaranteed.
[0065] The above-mentioned reference voltage Vr is generated by reference-voltage generation circuit Vref shown in drawing 34 . this reference-voltage generation circuit -- the last card row output of three steps of in-series inverters I341, I342, and I343 -- the first rank -- it is the circuit returned to the input and oscillation prevention processing by the grounding capacitance C34 and the balanced resistances R341 and R342 is performed like the above-mentioned addition section It is completed as the stable point that the I/O voltage becomes equal by the output, and reference-voltage generation circuit Vref can generate a desired reference voltage by threshold setup of each MOS inverter. In order to secure a sufficiently big dynamic range to positive/negative both directions generally, it is set up in many cases with Vr=Vdd/2.

Vdd is the supply voltage of MOS inverter here.
[0066] Drawing 35 shows the 2nd example of a multiuser demodulator, rather than drawing 17 , raises the proportion of an analog circuit and has analog-ized further the principal wave extraction circuit and the re-diffusion circuit.
[0067] Drawing 36 shows the 1st example of the analog type principal wave extraction circuit TH11. The principal wave extraction circuit TH11 consists of comparator CMP36, and the input voltage Vin36 and the threshold voltage Vth are inputted into the input. The voltage V1 of a high level and the voltage V2 of a low are impressed to CMP36, and when it is Vin36 >=Vth, at the time of Vin36<Vth, V2 becomes [V1] the output of CMP36. Drawing 37 is a graph which shows the input/output relation of CMP36, and output voltage Vout36 is changing from V1 to V2 abruptly by whether input voltage Vin exceeds Vth. By this, the fraction which surpassed the threshold voltage in the ******** VCF output is set to V1, and other fractions are set to V2. The result which processed the ******** VCF output of drawing 2 by the above principal wave extraction circuit becomes as in drawing 38 , and it turns out that the wave motion power of choice is extracted. In addition, it cannot be overemphasized that TH12 - TH1n can be constituted similarly.

[0068] Drawing 39 shows the 2nd example of the principal wave extraction circuit TH11. The principal wave extraction circuit TH11 has the multiplexer MUX39 into which input voltage and the above-mentioned reference-voltage Vref were inputted, and the signal of the result which subtracted the threshold voltage Vth from Vin39 as a control signal of a multiplexer is used. Vth is inputted into the three step inverters I391, I392, and I393 as an inversion buffer through capacitance C391, and the output of I393 has returned to the input of I391 through capacitance C392. Moreover, the grounding capacitance C393 is connected to I393 output, and the balanced resistances RE391 and RE392 are connected to I392 output. I393 output and Vin36 are inputted into capacity-coupling CP39 which consists of capacitance C394 and C395, and the output of CP39 is inputted into the inverter I394. The above-mentioned three step inverter generates the inversion output of Vth with a good alignment property, and capacity-coupling CP39 generates the sum of the output of I393, and Vin39. Here, it becomes if the output of CP39 is set to Vo39 and C394=C395.
[Equation 11]

$$Vo39 = \frac{C394(Vdd - Vth) + C395 \cdot Vin39}{C394 + C395} = \frac{Vdd}{2} + \frac{Vin39 - Vth}{2} \qquad (16)$$

[0069] An inverter I394 outputs OV, when Vdd / two or more voltages are inputted (i.e., when it is Vin39 >=Vth), and it outputs Vdd at the time of Vin39<Vth. MUX39 is controlled by the signal binary [this]. MUX39 outputs Vin39 at the time of Vin39 >=Vth, and outputs Vref at the time of Vin39<Vth. Therefore, the result which processed the ******** VCF output of drawing 2 by the principal wave extraction circuit is as drawing 40 . In addition, it cannot be overemphasized that TH12 - TH1n can be constituted like TH11.
[0070] Drawing 41 shows the 1st example of re-diffusion circuit RS11. In RS11, input voltage Vin41 is connected to a switch SW41, and it is opened [SW41] and closed by the control signal CTRL41 in suitable timing. The output of SW41 is inputted into the three step inverters I411, I412, and I413 as an inversion buffer through capacitance C411, and the output of this three step inverter is inputted into the same three step inverters I414, I415, and I416 through capacitance C414. The output of I413 returns to the input of I411 through capacitance C412, and the output of I416 has returned to the input of I414 through capacitance C415. The grounding capacitance C413 and C416 is connected to the output of I413 and I416, respectively, and the balanced resistances RE411, RE412, RE413, and RE414 are connected to the output of I412 and I415.
[0071] The output of I413 and I416 is inputted into a multiplexer MUX41, and MUX41 is switched and controlled by the binary PN code. When a PN code is "1", the output of I416 is chosen, and noninverting Vin41 which passed through the inversion buffer of two phases is outputted from MUX41. Moreover, when a PN code is "-1" or "0", the output of I413 is chosen, and the inversion signal of Vin41 which passed through the inversion buffer of one phase is outputted from MUX41. The output Vout41 of MUX41 is equivalent to the result which multiplied input voltage Vin41 by the PN code, and this serves as the diffusion signal of Vin41. In addition, since RS12 - RS1n are the same as that of RS11, they omits an explanation.
[0072] Drawing 42 shows the 2nd example of re-diffusion circuit RS11, and comes to connect the same circuit as drawing 26 with the latter part of the same sample hold circuit SH191 as drawing 20 . A sample hold circuit carries out the series connection of a buffer B421, the switch SW421, the buffer B422, the switch SW422, and the buffer B423, and comes to connect the grounding capacitance C421 and C422 with the output of SW421 and SW422. The output of B423 is connected to the switch SW423 of 1 input 2

output, and the 1st output is inputted into the inversion buffer which consists of an impedance C423, an operational amplifier OP42, and feedback capacitance C42. The output of this inversion buffer is Vout421. Moreover, the 2nd output of SW243 is considered as the output Vout422 as it is. In suitable timing, this is reversed with an inversion buffer or input voltage Vin42 is outputted, without being reversed, once holding by the sample hold circuit.

[0073]

[Effect of the Invention] The extracted signal is re-diffused, the multiuser recovery technique which starts this invention as above-mentioned extracts a specific user's signal by only carrying out threshold processing of the signal which carried out back-diffusion of gas of the input signal, since the input signal for a specific user is extracted by reducing re-diffusion signals other than a specific user from an input signal, the trouble relevant to the synchronization is canceled conventionally, and it has the outstanding effect that an interference canceller is unnecessary.

[Translation done.]

Field

[Field of the Invention] this invention relates to the multiuser demodulator for the receiver of a base station in a spectrum diffusion communication of a DS-CDMA (Direct Sequence-Code Division Multiple Access) method.

[Translation done.]

Technique

[Description of the Prior Art] Although the separation extraction of each user's signal needed to be carried out and back-diffusion of gas of the extracted signal needed to be carried out in the base station receiver of a DS-CDMA method spectrum diffusion communication, having received the signal from two or more users, and taking an interference etc. into consideration, the correlation operation for back-diffusion of gas was performed in many cases using slide ********** (it is called below Sliding Correlator:SC) which consists of a former comparatively simple circuit. And it was required that the phase simulation of the diffusion sign of an input signal and the diffusion sign of a receiver was perfect, and synchronous usurpation and holding circuits, such as DLL (DelayLocked Loop), were required for SC. However, since it was difficult for DLL to have the fault that initial drawing-in time and re-drawing-in time are size, and to realize a perfect synchronization generally, the degradation of the receiving property by the imperfection of a synchronization arose.
[0003] Although the interference canceller was conventionally used in order to prevent the interference between each user's signals furthermore After this interference canceller passes through processing of the back-diffusion of gas of an input signal, rake synthesis, etc. Although the input signal for a specific user was extracted by reproducing the input signal corresponding to each user's signal, and reducing the reproduction signal of users other than a specific user from an input signal by spectrum diffusion, the circuit was very large-scale and expensive.

[Translation done.]

Effect

[Effect of the Invention] The extracted signal is re-diffused, the multiuser recovery technique which starts this invention as above-mentioned extracts a specific user's signal by only carrying out threshold processing of the signal which carried out back-diffusion of gas of the input signal, since the input signal for a specific user is extracted by reducing re-diffusion signals other than a specific user from an input signal, the trouble relevant to the synchronization is canceled conventionally, and it has the outstanding effect that an interference canceller is unnecessary.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] It aims at having been originated that such a conventional trouble should be canceled, and this invention canceling the trouble relevant to the synchronization, and an interference canceller offering the unnecessary multiuser recovery technique and unnecessary equipment.

[Translation done.]

MEANS

[Means for Solving the Problem] The multiuser recovery technique concerning this invention extracts a specific user's signal by only carrying out threshold processing of the signal which carried out back-diffusion of gas of the input signal, re-diffuses the extracted signal and extracts the input signal for a specific user by reducing re-diffusion signals other than a specific user from an input signal.
[0006]
[Embodiments of the Invention] Next, one example of the multiuser recovery technique concerning this invention is explained based on a drawing.

[Translation done.]

EXAMPLE

[Example] Drawing 1 shows notionally one example of the multiuser recovery technique concerning this invention, carries out back-diffusion of gas of the input-signal R (t) in complex ******** VCFs MF11 and MF12, ..., MF1n, and extracts each user's signal. Each user's signal extracted here has received asymmetry by the transmission line, and thermal noise is further included in the input signal. When ai and each user's diffusion sign are set to PNi and thermal noise is set [the signal of each user who took transmission-line asymmetry into consideration here] to n (t) for Ii (t) and its receiving level, input-signal R (t) is [Equation 1].

$$R(t) = a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \ldots + an \cdot PNn \cdot In(t) + n(t) \qquad (1)$$

It is expressed.

[0008] For example, if input-signal R (t) is processed by 1st ******** VCF MF11, the output voltage of the solid line of drawing 2 arises, and two or more peaks P1, P2, and P3 have appeared in this output voltage at every one period (1 symbol time). The voltage shown as a solid line is the correlation result of an operation of the 1st term of a formula (1) and a thermal-noise term, and the 1st-user diffusion sign. Moreover, an alternate long and short dash line is an interference-wave voltage, and is the correlation result of an operation of the sum of the 2nd term of a formula (1), - the n-th term, and the 1st-user diffusion sign.

[0009] Generally, although the diffusion sign given to each user has a high orthogonality, and the level of an interference wave is low since a cross-correlation is low, if the number of users increases, the level of an interference wave will become high as shown in drawing 2 , and an exact peak detection will become difficult in a DS-CDMA method.

[0010] Then, the output of ******** VCF MF11 - MF1n is inputted into the principal wave extraction sections TH11 and TH12, ..., TH1n, and removes an interference wave and thermal noise compulsorily. It is processing which a principal wave extraction is processing] threshold processing, and the inside P3 of the peaks P1-P3 in drawing 2 is notionally eliminated [processing] as a peak below predetermined level here, and produces a wave as shown in drawing 3 . However, in actual threshold processing, since the input below a threshold is changed into the signal of a low, the output of the drawing 38 or the drawing 40 produces it in fact. The principal wave extraction section makes a threshold the voltage which applied predetermined proportion to the peak voltage which gives the maximum power within 1 symbol time, and carries out threshold processing of the input signal. The output of the principal wave extraction section is inputted into the re-diffusion sections RS11 and RS12, ..., RS1n, respectively, and a spread spectrum is performed again. This re-diffusion output is the replica signal approximated to the input signal for each user, for example, the output of RS11 is a replica signal for users other than the 1st.

[0011] The diffusion signal for each user is generated using the above replica signal. That is, in generation of the diffusion signal for the i-th user, the sum of the replica signal of users other than the i-th is subtracted from input-signal R (t) in adder ADD1i. Input-signal R (t) is delayed by the delay circuit D1, and the timing with the processing result by the ******** VCF, the principal wave extraction section, and the re-diffusion circuit is adjusted. Supposing the status with an ideal replica signal, i.e., the i-th term of a formula (1), is extracted, an adder output will serve as the diffusion signal component for the i-th user, and the sum of thermal noise, as shown in a formula (2).

[Equation 2]

$$\begin{aligned} Aouti &= R(t) - \{a1 \cdot PN1 \cdot I1(t) + a2 \cdot PN2 \cdot I2(t) + \ldots + ai-1 \cdot PNi-1 \cdot Ii-1(t)\} \\ &\quad - \{ai+1 \cdot PNi+1 \cdot Ii+1(t) + \ldots + an \cdot PNn \cdot In(t)\} \\ &= ai \cdot PNi \cdot Ii(t) + n(t) \end{aligned} \qquad (2)$$

In the output of an adder, it turns out that the influence of a cross-correlation, i.e., an interference, can be mitigated so that clearly from a formula (2).
[0012] Thus, the correlation operation of the extracted diffusion signal component is carried out by complex ******** VCFs MF21 and MF22, ..., MF2n, and, ideally, the back-diffusion-of-gas signal component of each user in an input signal is extracted. In the judgment circuits J11 and J12, ..., J1n, presence of a correspondence user's signal is judged to this correlation result of an operation, and the signal is outputted.
[0013] Here, the effect of the example of drawing 1 is shown through various ******** VCF outputs when the multi-pass has not arisen.
[0014] Drawing 4 shows the example of a simulation of the output of above-mentioned ******** VCF MF21 when there are very few interferences. The conditions of a simulation are made into primary modulation QPSK, a diffusion sign 128 chip M sequence, the exaggerated measurement size 4, and two user numbers here, and it is a correlation operation under the static conditions in a baseband band. In this drawing, the 1st user's (it considers as the office of choice.) correlation peak is detected at the time of t= 0. Moreover, 100dB and the wave motion power pair interference-wave power ratio (D/U) of choice of the signal energy pair noise power flux density per bit (Eb/No) are 100dB, and the influence of a noise and an interference performed parvus conditioning extremely. In addition, the peak in time t= 512 is unrelated to the impulse response of a transmission line according to the contiguity symbol.
[0015] Drawing 5 is what carried out 16 symbol time display of the ******** VCF output of drawing 4 , and shows simultaneously the real-number component (I phase) and the imaginary number component (Q phase). Therefore, when there is only one peak, I phase and Q phase have the same polarity, and that a peak exists up and down shows that I phase and Q phase are an antiphase mutually. As shown in drawing, on such ideal conditions, a clear peak arises and the interference by other users is not produced.
[0016] Drawing 6 is as a result of [which ten interference offices other than D/U=-10dB, i.e., the office of choice, exist, and shows the status of =(wave motion power of choice)0.1x (interference-wave power)] a simulation. Here, the big interference peak other than the office peak of choice of t= 0 is produced at the time of t= 270. It is generated when it differs if a diffusion sign changes, since it is influenced by the cross-correlation value, and this interference peak causes an incorrect judging. Or the office peak level of choice may decline by presence of an interference peak, and it is easy to produce an incorrect judging also at this point.
[0017] Drawing 7 is a ******** VCF output for interference offices in the same conditions as drawing 6 , and the interference office peak has produced it more clearly than the office peak of choice of drawing 6 . Although it is the position of this peak at the time of t= 128, it is based on this having adopted the method of asynchronous CDMA. With asynchronous CDMA, each user's diffusion sign is made asynchronous into the same cell here. The diffusion sign phase of an interference wave is shifted as the worst conditions this time by 128 samples which become the worst [a cross-correlation value] (a part for 32 chips).
[0018] Drawing 8 carries out 16 symbol term display of the ******** VCF output of drawing 6 . In this case, the office peak of choice which should be produced in t= 0 is unstable, and the detection is impossible. That is, it also understands a certain thing that the office of choice is buried with some level of a cross-correlation value.
[0019] In the comparison with the above graph, the result which removed the interference wave according to the example of drawing 1 is shown in drawing 9 . That is, drawing 9 shows the result which removed the interference wave according to the example of drawing 1 , the peak of the office of choice is stabilized, and the almost same property as the case (drawing 5) where an interference wave does not exist is acquired. That is, elimination of an interference wave can detect the office peak of choice now certainly.
[0020] Next, the case where a multi-pass arises is explained.
[0021] Drawing 10 is a ******** VCF output when carrying out 3 pass static conditions of the impulse response of a transmission line, the direct wave of the office of choice arises in t= 128, and the retardation wave motion has produced it in t= 138 and t= 148. here -- the gain of each pass -- 1.0 and 0. -- it is set as 7 and 0.5
[0022] drawing 11 -- the multi-pass signal of drawing 10 -- Eb/No=100dB (there is almost no influence of a noise.), and D/U=-10dB (the influence of an interference wave is large.) -- the ******** VCF output of 16 symbol time is displayed on the bottom of conditions in this drawing, since interference-wave level is high, the peak of the office of choice can be recognized -- it has become
[0023] Drawing 12 performs interference cancel by the example of drawing 1 to the same multi-pass signal as drawing 11 , and the direct wave of the office of choice serves as a clear peak, it appears, and it turns out that it can perform a peak detection certainly.

[0024] Drawing 13 is a graph which shows the bit error rate to Eb/NO variously, and compares the bit error rate (a dashed line and a balloon plot show.) by the example of drawing 1 , the bit error rate (dashed line) when not performing interference-wave cancel at all, and a bit error rate theoretical value (solid line). When not performing interference-wave cancel from drawing, as compared with this example, a bit error rate increases several 10 times from several times, and this example serves as the value approximated to the theoretical value.
[0025] Processing of complex ******** VCF MF11 in the example of drawing 1 - MF1n, MF21-MF2n, the principal wave extraction section TH11 - TH1n, re-diffusion section RS11 - RS1n, adder ADD11 - ADD1n, and the judgment circuit J11 - J1n is realizable with various modes so that it may illustrate below.
** The mode which realized the whole by software on the general purpose computer.
** For CPU, it is the mode which realized only the ******** VCF with a high calculation load by DSP or the digital circuit of exclusive use, and realized other fractions by software.
** The mode which realized the whole by DSP or the digital circuit of exclusive use.
** For CPU, it is the mode which realized only the ******** VCF with a high calculation load by the analog circuit, and realized other fractions by software.
** The mode which realized only the ******** VCF by the analog circuit and realized other fractions by DSP or the digital circuit of exclusive use.
** The mode which realized the whole by the analog circuit.
In order to raise processing speed, it is necessary to raise the proportion of an analog or a digital personal circuit and, and in these modes, the analog circuit is more advantageous than the digital circuit in respect of power consumption.
[0026] Drawing 14 shows ******** VCF MF11 by the exclusive digital circuit, and drawing 15 shows the principal wave extraction section TH11 by the exclusive digital circuit.
[0027] In drawing 14 , ******** VCF MF11 has shift register SFTREG of n stage where the digitized input signal Vin14 is inputted, and the multiplication circuit MUL141 - MUL14n are connected to each stage of a shift register, respectively. The PN code is set to each multiplication circuit as a multiplier, and the operation which multiplies by the PN code to an input signal is performed. And all the outputs of a multiplication circuit are inputted into adder-circuit ADD14, and are integrated in here. The addition result Vout14 is the so-called ******** VCF output. In addition, since a PN code is usually 1-bit data, the AND gate which passes each bit of an input signal is sufficient for a multiplication circuit.
[0028] The principal wave extraction circuit TH11 has shift register SFTREG which holds the ******** VCF output Vin15 by 1 symbol time, and comparator circuits C1-Cn are connected to each stage of this shift register. the first rank of a shift register -- a stage is connected to the maximum circuit MAX and the feedback data from the latter multiplexer MUX are inputted into this maximum circuit The output of the maximum circuit MAX is connected to registers REG1 or REG2 through a selector SEL, and a multiplexer MUX outputs the output of these registers alternatively. the data with which the maximum circuit was outputted from MUX, and the new first rank -- stage data are compared and larger data are inputted into a new register When the data outputted here from MUX are a thing from REG1, REG2 serves as a new register and serves as the register with new REG1 to REG2. Therefore, large data will be registered into REG1 and REG2 by alternation. A selector is switched to a register always new and a multiplexer is switched in response to this.
[0029] The output of a multiplexer is further connected to the multiplication circuit MUL, and the threshold Vth which applied predetermined proportion to maximum here is computed. The threshold computed here is inputted into comparator circuits C1-Cn, and is compared with the data of each stage of a shift register. The comparison result is as being shown in drawing 16 , only the data more than Vth are outputted as it is, and the data of under Vth are omitted by OV. Processing of the above-mentioned principal wave extraction is attained by this.
[0030] Drawing 17 shows one example of the demodulator concerning this invention, realizes the principal wave extraction section, the re-diffusion section, and a judgment circuit by the exclusive digital circuit, and has realized others by the exclusive analog circuit.
[0031] In drawing 17 , input-signal R (t) is inputted into ******** VCF MF11 - MF1n, and the delay circuit D17 of an analog, and the output of MF11 - MF1n passes through A/D-conversion circuit ADC11 - ADC1n, and is inputted into the digital principal wave extraction circuit TH11 - TH1n, and re-diffusion circuit RS11 - RS1n. The output of RS11 - RS1n is inputted into adder-circuit ADD11 - ADD1n through D/A-conversion circuit DAC11 - DAC1n, and is subtracted from the output of a delay circuit D17. The output of an adder circuit is inputted into ******** VCF MF21 - MF2n, and is again inputted into the judgment circuit J11 - J1n through A/D-conversion circuit ADC21 - ADC2n after that.

[0032] drawing 18 -- setting -- the analog delay circuits D181 and D182 of a plurality [MF / ******** VCF /11 / of an analog], ..., D18n -- in-series -- connecting -- input-signal R (t) of an analog -- the first rank -- it is transmitted to the latter part one by one from a delay circuit, and results in last card row delay circuit D18n The analog multiplication circuit MUL181, ..., MUL18n are connected to the output of each delay circuit, and PN codes PN1, PN2, ..., PNn are hung on an input signal in these multiplications circuit. The output of the multiplication circuit MUL181 - MUL18n is inputted into adder-circuit ADD181, and all multiplication results are added. If delay time in the delay circuit D181 - D18n is set to Tc, the following operations will be performed with the above ******** VCF.
[Equation 3]

$$S(t)=\sum_{i=1}^{n} PNi \cdot R(t-i \cdot Tc) \qquad (3)$$

In addition, the above configuration is the same also about MF12 - MF1n, and MF21-MF2n.

[0033] drawing 19 -- setting -- the sample hold circuit SH191 of a plurality [delay circuit / D17], - SH19n -- in-series -- connecting -- the first rank -- the input voltage Vin19 inputted into the sample hold circuit SH191 is transmitted to the latter part one by one, and each sample hold circuit performs sample hold of data in response to a clock CLK19 The number of stages of a delay circuit and the timing of a clock are set up so that it may synchronize with the timing to which input-signal R (t) arrives at an adder circuit through a ******** VCF, the principal wave extraction section, and the re-diffusion section. In addition, it is also possible for a delay circuit to have the function of a shift register and to use the output Vout191 from each sample hold circuit - Vout19n as data as it is. In addition, the analog delay circuit in drawing 18 also becomes the same configuration as drawing 19 .
[0034] A sample hold circuit SH191 is constituted as shown in drawing 20 , it connects a buffer B201, the switch SW201, the buffer B202, the switch SW202, and the buffer B203 to a serial one by one, and comes to connect the grounding capacitance C201 and C202 with the latter part of switches SW201 and SW202. Input voltage Vin20 is inputted into a buffer B201, and a buffer outputs Vin20 stably irrespective of a latter load. When SW201 is closed, the charge and discharge of the grounding capacitance C201 will be carried out to the charge corresponding to the output voltage of a buffer B201, and a voltage will be held with capacitance C201. After the completion of a hold, a switch SW201 is opened wide and a hold of the following input voltage is equipped with it. The held voltage turns into the input voltage of a buffer B202, and is stably outputted from a buffer B202. If a switch SW202 is closed here, according to the output voltage of a buffer B202, the charge and discharge of the grounding capacitance C202 will be carried out, and the output of a buffer B202 will be held. The voltage held with the grounding capacitance C202 turns into the input voltage of a buffer B203, and is outputted to the latter part as a stable output Vout20 of a buffer B203.
[0035] Switches SW201 and SW202 are closed by turns to predetermined timing, and input voltage Vin20 is transmitted and held one by one C201 and C202. And since the voltage transmitted to C202 is not influenced of input voltage Vin20 to closing of the next switch SW202, it can generate the stable output Vout20.
[0036] As a buffer B201, a ********** follower type (drawing 21) or an inversion buffer type (drawing 22) can be adopted.
[0037] A buffer B201 connects input voltage Vin21 to the noninverting input of an operational amplifier OP21, and makes output voltage Vout21 come to return to the inversion input in drawing 21 . In this circuit, the ratio of I/O is set to +1 and an input arises in an output as it is.
[0038] The circuit of drawing 22 grounds the noninverting input of an operational amplifier OP22, and comes to connect input voltage Vin22 with an inversion input through an impedance Z221. Moreover, the output of an operational amplifier OP22 has returned to the inversion input through the impedance Z221 and the equal impedance Z222. The output Vout22 of this circuit is equal to -Vin22, and since input voltage is outputted in a sample hold circuit through three steps of buffers B201, B202, and B203, the final output is inverted. Therefore, although the final output Vout19 (drawing 19) serves as the same sign as Vin19 when the sample hold circuit in a delay circuit is even level, at the time of odd level, you should add the buffer for reversing an input or an output further. In addition, since the sample hold circuit SH192 - SH19n are constituted like SH191, they omits an explanation.
[0039] Drawing 23 is a graph which shows an operation of a sample hold circuit, and shows input voltage (Vin20), the 2nd step buffer (B202) output, and output voltage (Vout20) in the relation with a clock CLK20 about SH191 and SH192.

[0040] If a switch SW201 is closed in Vin20 to SH191 changing now (CLK20 is a low), Vin20 will appear as B202 output of SH191 as it is during the closed period. B202 output is fixed until B202 output is held and CLK20 is again set to a low, when SW201 is opened (CLK20 is a high level). A switch SW202 is closed at the time of the high level of CLK20, generates the voltage which held the voltage held at the time of SW201 opening one by one by one period of CLK20, and outputs it as Vout20.
[0041] The output of a sample hold circuit SH191 serves as the input voltage (Vin20) of the 2nd step of sample hold circuit SH192, is held in SH192 to the timing for which CLK20 was delayed by the half period in input voltage by SW201, generates the voltage which carried out the half-period retardation of it further by SW202, and outputs it as output voltage Vout20.
[0042] As compared with a digital type delay circuit, a circuit scale is small, and the delay circuit above analog type has slight power consumption.
[0043] Drawing 24 shows the 2nd example of a sample hold circuit. This sample hold circuit realizes the same property as an inversion buffer by three steps of CMOS inverters I241, I242, and I243, the output of I243 returns to the input of I241 through the feedback capacitance C242, and input voltage Vin24 is connected to the input of I241 through the CMOS switch SW241 and the input capacitance C241 one by one.
[0044] If it is wide opened once SW241 is closed, the charge and discharge of C241 will be carried out to the charge according to Vin24 at the time. C242 is set up equally to C241, and the three step inverters I241-I243 output the voltage held by C241 as an output of I243 as it is. The CMOS switch SW242 is connected to the output of I243; and the hold of input voltage and the output are possible by opening and closing SW241 and SW242 by turns like the sample hold circuit of drawing 20 .
[0045] Furthermore, an output is inputted into SW242 through capacitance C244 at the same three step CMOS inverters I244, I245, and I246 as the above, and the output of I246 is connected to the input of I244 through the feedback capacitance C245. The sign of I/O of a sample hold circuit has consistency by this.
[0046] The grounding capacitance C243 and C246 as a low pass filter is connected to the output of a last card row MOS inverter, and, as for these three steps inverter, one pair of balanced resistances RE241, RE242, RE243, and RE244 are connected to the 2nd step of output. RE241 and RE243 are connected to supply voltage Vdd, and RE242 and RE244 are grounded and have suppressed the gain of a three step inverter. By such circuit arrangement, the oscillation of the three step inverter containing the feedback system is prevented.
[0047] Drawing 25 shows the multiplication circuit of above-mentioned ******** VCF MF11, leads input voltage Vin25 to the impedances Z251 and Z252 from which a plurality is different, ..., Z25n, and has inputted the output of these impedances into the inversion input of an operational amplifier OP25 in arbitrary combination by the switch SW251 - SW25n. A noninverting input is grounded and, as for the operational amplifier OP25, the output has returned to the inversion input through feedback-impedance Z25f. An operational amplifier OP25 constitutes an inversion buffer, and each impedance consists of a capacitor. Impedance Z25i is [Equation 4] by capacitor C25i here.

$$Z25i = \frac{1}{j\omega C25i} \qquad (4)$$

When the sum of the capacity of the capacitor by which it was expressed and the switch was closed is expressed as sigmaC25i, output voltage Vout25 is [Equation 5].

$$Vout25 = -\frac{\sum C25i}{C25f} Vin25 \qquad (5)$$

It becomes. This means the multiplication which multiplied by - (C25i/C25f) to Vin25. If SW251 - SW25n are closed in arbitrary combination, for example, the capacity of C25i is set as the exponentiation of 2, the multiplication of the arbitrary multipliers of a binary digit will become possible. in addition, a PN code -- as for such a weighting, or (1, 0) (1, -1) is unnecessary at the time of binary
[0048] In addition, as shown in a formula (5), since it is reversed, when using this as an output as it is, the inversion buffer which reverses a sign further is required for the sign of an output. Moreover, the sign of a coefficient is not contained in the formula (5). Drawing 26 is an addition circuit for this inversion or sign adjustment, and according to the sign of a multiplier (PN code), Vout25 is led to an inversion buffer, or it carries out a direct output. An inversion buffer grounds a noninverting input while it connects an impedance Z26 to the inversion input of an operational amplifier OP26, and it is returning the output of OP26 to the inversion input. The output Vout261 which went via the inversion buffer corresponds to a positive PN code, and a direct output Vout262 corresponds to a negative PN code.

[0049] Drawing 27 shows adder-circuit ADD181 kicked to ******** VCF MF11. Adder-circuit ADD181 grounds a noninverting input, and is returning the output of an operational amplifier OP27 to the inversion input through impedance Z27f further while it connects the impedance Z271 - Z27n in parallel with the inversion input of an operational amplifier OP27. It is [Equation 6], when an impedance consists of capacitor C27i - C27n and C27f, and the input to each impedance is set to Vin271 - Vin27n and it sets an output to Vout27.

$$Vout27 = -\frac{\sum_{i=1}^{n} Vin27iC27i}{C27f} \qquad (6)$$

[0050] Drawing 28 shows ******** VCF MF11 for the binary PN code of (1, 0), ******** filter circuit MF11 has the sample hold circuit SH281 of a plurality (n pieces), - SH28n, and the parallel input of the input signal Vin28 is carried out at these sample hold circuits.
[0051] A sample hold circuit SH281 is constituted as shown in drawing 29 , and input voltage Vin29 is connected to the switch SW29. The output of a switch SW29 is connected to capacitance C291, and three steps of in-series MOS inverters I291, I292, and I293 are connected to the output of capacitance C291. It connects with the input of I291 through the feedback capacitance C292, and Vin29 produces the output Vo29 of the MOS inverter I293 of the last card row in the output of I293 with a good linearity by this. If SW29 is closed, C291 will be charged by the charge corresponding to Vin29, and the alignment property of an output will be guaranteed by the feedback function of I291-I293. And when a switch SW29 is opened wide after that, a sample hold circuit SH281 will hold Vin29. The output of I293 of the last card row is connected to a gland through the grounding capacitance C293, and the 2nd-step output of I292 is connected to the supply voltage Vdd and the gland through one pair of balanced resistances R291 and RE292. By such configuration, the oscillation of the inversion amplifying circuit containing the feedback system is prevented. In addition, since the sample hold circuit SH282 - SH28n are constituted like SH281, they omits an explanation.
[0052] As shown in drawing 30 , the above-mentioned multiplication circuit MUL11 consists of two multiplexers MUX301 and MUX302, and the above Vo29 and the common reference voltage Vr are connected to these multiplexers.
[0053] Switch SW and the multiplexers MUX301 and MUX302 are controlled by the control signals S1, S2, and S3, and once closing S1, when it should incorporate input voltage, it opens SW29. S2 and S3 are the inverted signals, and when one multiplexer outputs Vo29, the multiplexer of another side outputs Vr. MUX301 and MUX302 output Vo29 from MUX301, when it corresponds to "1" (high level) of a diffusion sign, and "-1" (low) and the input voltage at a certain time should be multiplied by the sign "1", and when it should multiply by "-1", they output Vo29 from MUX302. Since this highness and the level of a row are represented, in drawing 30 , VH and the output of MUX302 are displayed for the output of MUX301 by VL.
[0054] As shown in drawing 31 , a switch SW29 consists of a transistor circuit T31 which connects the source of n type MOS transistor, and a drain with the drain of p type MOS transistor, and the source, respectively, and becomes, connects input voltage Vin31 to the terminal by the side of the drain of nMOS of this transistor circuit, and comes to connect the terminal of the source of nMOS with an output terminal Vout31 through the dummy transistor DT31 of the same configuration. S1 is inputted into the gate of nMOS transistor in a transistor circuit T31, and the signal which inverted S1 by the inverter I31 is inputted into the gate of pMOS transistor. When S1 is high-level, T31 flows, and T31 is intercepted by this when it is a low.
[0055] As shown in drawing 32 , the drain of one pair of MOS transistors of n type and p type [multiplexer / MUX301], In the terminal by the side of the drain of nMOS [in / it comes to connect with the common output terminal Vout32 the terminal by the side of the source of nMOS of the transistor circuits T321 and T322 which come to connect the source mutually, and / T321], it is the output Vo29 (it is shown all over [Vin321] drawing.) of the MOS inverter I293. It connects and is a reference voltage Vr (it is shown all over [Vin322] drawing.) in the drain of T322. It connects. A signal S2 is inputted into the gate of nMOS transistor in a transistor circuit T321, and the gate of pMOS transistor in a transistor circuit T322, and the signal which inverted S2 by the inverter I32 is inputted into the gate of nMOS of pMOS and T322 of T321. When S2 is high-level, T321 flows, T322 is intercepted by this, T322 flows at the time of a low, and T321 is intercepted. That is, MUX301 may output Vo29 or Vr alternatively with control of S2.
[0056] Although illustration is omitted, a multiplexer MUX302 is constituted like MUX301, and connection of Vo29 and Vr has reversed it. That is, it is the configuration of having connected Vr to T321 and having connected Vo3 to T322. By this, MUX302

outputs Vo29, when the output 301 opposite to MUX301, i.e., MUX, outputs Vo29 and MUX301 outputs Vr for Vr.
[0057] A signal S2 corresponds to a diffusion sign, and when S2 is "1", the multiplication circuit MUL11 outputs Vr and MUX302 to Vo29 from MUX301, when S2 is "0" about Vo29 and MUX302 to Vr from MUX301. These outputs are led to above-mentioned adder-circuit ADD28. That is, although the signal of one line from MUL281 to ADD28 is described, this represents two signals, a high-level side and a low side, with drawing 28 .
[0058] In drawing 33 , adder-circuit ADD28 has the capacity coupling CPL as which the low signals VL1-VLn from the capacity coupling CPH and MUL281 - MUL28n into which the high-level signals VH1-VHn from MUL281, MUL282, ..., MUL28n were inputted were inputted, CPL comes to carry out parallel connection of the capacitance CL1-CLn, and CPH comes to carry out parallel connection of the capacitance CH1-CHn. the first rank of the MOS inverters I331, I332, and I333 with the output of CPL in-series three steps -- it connects with an input -- having -- the output of I333 -- the feedback capacitance C331 -- minding -- the first rank -- it is fed back to the input This three step inverter has guaranteed the linearity of input/output relation according to sufficient big its open loop and gain.
[0059] the first rank of the MOS inverters I334, I335, and I336 with the output of CPH in-series three steps -- it connects with an input -- having -- the output of I336 -- the feedback capacitance C333 -- minding -- the first rank -- it is fed back to the input This three step inverter has guaranteed the linearity of input/output relation according to sufficient big its open loop and gain. Furthermore, the output of I333 is connected to the input of I334 through joint capacitance CC33 in parallel with capacity coupling CPH, and the sum of inversion of the output of CPL and the output of CPH is inputted into the three step inverters I334-I336.
[0060] The output of the MOS inverters I333 and I336 of the last card row in the above-mentioned three step inverter is connected to a gland respectively through the grounding capacitance C332 and C334, and the output of the 2nd step of MOS inverters I332 and I335 is connected to the supply voltage Vdd and the gland respectively through one pair of balanced resistances R331, R332, R333, and R334. By such configuration, the oscillation of the inversion amplifying circuit containing the feedback system is prevented.
[0061] Adder-circuit ADD28 performs the operation of a formula (7), and since the relation between capacitance is set up like formula (8) - (10), the formula (11) result of an operation is obtained as a result.
[Equation 7]

$$Vout33 = Vdd - \frac{\left(Vdd - \frac{\sum_{i=1}^{n} VLi \cdot CLi}{C331} \right) \cdot CC33 + \sum_{i=1}^{n} VHi \cdot CHi}{C333} \qquad (7)$$

$$CL1 = CL2 = \ldots = CLn \qquad (8)$$

$$CH1 = CH2 = \ldots = CHn \qquad (9)$$

$$C331 = C333 = CC33 = n \cdot CLi = n \cdot CHi \qquad (10)$$

$$Vout33 = \frac{\sum_{i=1}^{n} (VLi - VHi)}{n} \qquad (11)$$

[0062] VLi and Vhi are changed into representation of the formula (12) on the basis of a reference voltage Vr, and (13) here.
[Equation 8]

$$VHi = Vr + vhi \qquad (12)$$

$$VLi = Vr + vli \qquad (13)$$

A formula (14) will be obtained if this formula (12) and (13) are substituted for a formula (11).
[Equation 9]

$$Vout33 = \frac{\sum_{i=1}^{n} (vli - vhi)}{n} \qquad (14)$$

[0063] Furthermore, a formula (14) is rewritten by the formula (15), when the signal which held the input signal Vin1 to time series by the sample hold circuit SH31 - SH3n when a certain time was set to t and chip time was set to Tc and natural number i sets to Pni S (t-i and Tc) and the PN code by which this is multiplied, since inversion of the data by the three step inverter is performed also in the sample hold circuit.
[Equation 10]

$$Vout33 = \frac{\sum_{i=1}^{n} PNi \cdot S(t - i \cdot Tc)}{n} \qquad (15)$$

This is the operation of a common ******** VCF.
[0064] In addition, since the output is normalized by number n of an input in the above operation, it is prevented that the maximum voltage of an output exceeds supply voltage, and the stability of operation is guaranteed.
[0065] The above-mentioned reference voltage Vr is generated by reference-voltage generation circuit Vref shown in drawing 34 . this reference-voltage generation circuit -- the last card row output of three steps of in-series inverters I341, I342, and I343 -- the first rank -- it is the circuit returned to the input and oscillation prevention processing by the grounding capacitance C34 and the balanced resistances R341 and R342 is performed like the above-mentioned addition section It is completed as the stable point that the I/O voltage becomes equal by the output, and reference-voltage generation circuit Vref can generate a desired reference voltage by threshold setup of each MOS inverter. In order to secure a sufficiently big dynamic range to positive/negative both directions generally, it is set up in many cases with Vr=Vdd/2. Vdd is the supply voltage of MOS inverter here.
[0066] Drawing 35 shows the 2nd example of a multiuser demodulator, rather than drawing 17 , raises the proportion of an analog circuit and has analog-ized further the principal wave extraction circuit and the re-diffusion circuit.
[0067] Drawing 36 shows the 1st example of the analog type principal wave extraction circuit TH11. The principal wave extraction circuit TH11 consists of comparator CMP36, and the input voltage Vin36 and the threshold voltage Vth are inputted into the input. The voltage V1 of a high level and the voltage V2 of a low are impressed to CMP36, and when it is Vin36 >=Vth, at the time of Vin36<Vth, V2 becomes [V1] the output of CMP36. Drawing 37 is a graph which shows the input/output relation of CMP36, and output voltage Vout36 is changing from V1 to V2 abruptly by whether input voltage Vin exceeds Vth. By this, the fraction which surpassed the threshold voltage in the ******** VCF output is set to V1, and other fractions are set to V2. The result which processed the ******** VCF output of drawing 2 by the above principal wave extraction circuit becomes as in drawing 38 , and it turns out that the wave motion power of choice is extracted. In addition, it cannot be overemphasized that TH12 - TH1n can be constituted similarly.

[0068] Drawing 39 shows the 2nd example of the principal wave extraction circuit TH11. The principal wave extraction circuit TH11 has the multiplexer MUX39 into which input voltage and the above-mentioned reference-voltage Vref were inputted, and the signal of the result which subtracted the threshold voltage Vth from Vin39 as a control signal of a multiplexer is used. Vth is inputted into the three step inverters I391, I392, and I393 as an inversion buffer through capacitance C391, and the output of I393 has returned to the input of I391 through capacitance C392. Moreover, the grounding capacitance C393 is connected to I393 output, and the balanced resistances RE391 and RE392 are connected to I392 output. I393 output and Vin36 are inputted into capacity-coupling CP39 which consists of capacitance C394 and C395, and the output of CP39 is inputted into the inverter I394. The above-mentioned three step inverter generates the inversion output of Vth with a good alignment property, and capacity-coupling CP39 generates the sum of the output of I393, and Vin39. Here, it becomes if the output of CP39 is set to Vo39 and C394=C395.
[Equation 11]

$$Vo39 = \frac{C394(Vdd - Vth) + C395 \cdot Vin39}{C394 + C395} = \frac{Vdd}{2} + \frac{Vin39 - Vth}{2} \qquad (16)$$

[0069] An inverter I394 outputs OV, when Vdd / two or more voltages are inputted (i.e., when it is Vin39 >=Vth), and it outputs Vdd at the time of Vin39<Vth. MUX39 is controlled by the signal binary [this]. MUX39 outputs Vin39 at the time of Vin39 >=Vth, and outputs Vref at the time of Vin39<Vth. Therefore, the result which processed the ******** VCF output of drawing 2 by the principal wave extraction circuit is as drawing 40 . In addition, it cannot be overemphasized that TH12 - TH1n can be

constituted like TH11.
[0070] Drawing 41 shows the 1st example of re-diffusion circuit RS11. In RS11, input voltage Vin41 is connected to a switch SW41, and it is opened [SW41] and closed by the control signal CTRL41 in suitable timing. The output of SW41 is inputted into the three step inverters I411, I412, and I413 as an inversion buffer through capacitance C411, and the output of this three step inverter is inputted into the same three step inverters I414, I415, and I416 through capacitance C414. The output of I413 returns to the input of I411 through capacitance C412, and the output of I416 has returned to the input of I414 through capacitance C415. The grounding capacitance C413 and C416 is connected to the output of I413 and I416, respectively, and the balanced resistances RE411, RE412, RE413, and RE414 are connected to the output of I412 and I415.
[0071] The output of I413 and I416 is inputted into a multiplexer MUX41, and MUX41 is switched and controlled by the binary PN code. When a PN code is "1", the output of I416 is chosen, and noninverting Vin41 which passed through the inversion buffer of two phases is outputted from MUX41. Moreover, when a PN code is "-1" or "0", the output of I413 is chosen, and the inversion signal of Vin41 which passed through the inversion buffer of one phase is outputted from MUX41. The output Vout41 of MUX41 is equivalent to the result which multiplied input voltage Vin41 by the PN code, and this serves as the diffusion signal of Vin41. In addition, since RS12 - RS1n are the same as that of RS11, they omits an explanation.
[0072] Drawing 42 shows the 2nd example of re-diffusion circuit RS11, and comes to connect the same circuit as drawing 26 with the latter part of the same sample hold circuit SH191 as drawing 20 . A sample hold circuit carries out the series connection of a buffer B421, the switch SW421, the buffer B422, the switch SW422, and the buffer B423, and comes to connect the grounding capacitance C421 and C422 with the output of SW421 and SW422. The output of B423 is connected to the switch SW423 of 1 input 2 output, and the 1st output is inputted into the inversion buffer which consists of an impedance C423, an operational amplifier OP42, and feedback capacitance C42. The output of this inversion buffer is Vout421. Moreover, the 2nd output of SW243 is considered as the output Vout422 as it is. In suitable timing, this is reversed with an inversion buffer or input voltage Vin42 is outputted, without being reversed, once holding by the sample hold circuit.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the idea of the equipment for carrying out one example of this invention technique.
[Drawing 2] It is the graph which shows the ******** VCF output in this example.
[Drawing 3] It is the graph which shows the wave motion power of choice.
[Drawing 4] It is the graph which shows a ******** VCF output when there are few interferences.
[Drawing 5] It is the graph which shows the ******** VCF output of a longer term in the same conditions as drawing 4 .
[Drawing 6] It is the graph which shows the ******** VCF output under presence of an interference office.
[Drawing 7] It is the graph which shows the ******** VCF output for the interference offices in the same conditions as drawing 6 .
[Drawing 8] It is the graph which shows the ******** VCF output of a longer term in the same conditions as drawing 6 .
[Drawing 9] It is the graph which shows a ******** VCF output after the example of drawing 1 removes an interference wave to the same input signal as drawing 6 .
[Drawing 10] It is the ******** VCF output of a multi-pass signal.
[Drawing 11] It is a ******** VCF output when adding the influence of an interference wave to the same multi-pass signal as drawing 10 .
[Drawing 12] It is the graph which shows a ******** VCF output after the example of drawing 1 removes an interference wave to the same input signal as drawing 11 .
[Drawing 13] When not performing interference-wave elimination for the bit error rate by the example of drawing 1 , it is a graph in comparison with a theoretical value.
[Drawing 14] It is the block diagram showing one example of the ******** VCF by the exclusive digital circuit.
[Drawing 15] It is the block diagram showing one example of the principal wave extraction circuit by the exclusive digital circuit.
[Drawing 16] It is the graph which shows the output of a principal wave extraction circuit.
[Drawing 17] It is the block diagram showing the demodulator which made the ******** VCF the analog circuit.
[Drawing 18] It is the block diagram showing the ******** VCF in drawing 17 .
[Drawing 19] It is the block diagram showing the delay circuit in drawing 17 .
[Drawing 20] It is the circuit diagram showing the sample hold circuit in drawing 19 .
[Drawing 21] It is the circuit diagram showing the 1st example of the buffer in drawing 20 .
[Drawing 22] It is the circuit diagram showing the 2nd example of the buffer in drawing 20 .
[Drawing 23] It is the timing chart which shows an operation of the 1st step and the 2nd step of sample hold circuit in drawing 19 .
[Drawing 24] It is the circuit diagram showing the 2nd example of a sample hold circuit.
[Drawing 25] It is the circuit diagram showing the multiplication circuit in the ******** VCF of drawing 18 .
[Drawing 26] It is the circuit diagram showing the circuit for processing a sign in this ******** VCF.
[Drawing 27] It is the circuit diagram showing the adder circuit in this ******** VCF.
[Drawing 28] It is the block diagram showing the 2nd example of an analog type ******** VCF.
[Drawing 29] It is the circuit diagram showing the sample hold circuit of drawing 28 .
[Drawing 30] It is the circuit diagram showing the multiplication circuit of drawing 28 .
[Drawing 31] It is the circuit diagram showing the switch of drawing 29 .

[Drawing 32] It is the circuit diagram showing the multiplexer of drawing 30 .
[Drawing 33] It is the circuit diagram showing the adder circuit of drawing 28 .
[Drawing 34] It is the circuit diagram showing the circuit for generating the reference voltage of drawing 30 .
[Drawing 35] It is the block diagram showing the 2nd example of a demodulator.
[Drawing 36] It is the circuit diagram showing the 1st example of an analog type principal wave extraction circuit.
[Drawing 37] It is the graph which shows the input-output behavioral characteristics of this principal wave extraction circuit.
[Drawing 38] It is the graph which shows the result which processed the ******** VCF output of drawing 2 in this principal wave extraction circuit.
[Drawing 39] It is the circuit diagram showing the 2nd example of an analog type principal wave extraction circuit.
[Drawing 40] It is the graph which shows the result which processed the ******** VCF output of drawing 2 in this principal wave extraction circuit.
[Drawing 41] It is the circuit diagram showing the 1st example of a re-diffusion circuit.
[Drawing 42] It is the circuit diagram showing the 2nd example of a re-diffusion circuit.
[Description of Notations]
ADD11, ..., ADD1 -- n and ADD181 ... adder circuit
ADC11, ..., ADC1 -- n, ADC21, ..., ADC2n ... A/D converter
B201, B203, and B203 ... buffer
DAC11, ..., DAC1n ... D/A converter
D ... Delay circuit
D181, ..., D18n ... delay circuit
J11, ..., J1n ... Decision circuit
MF11, ..., MF1n ... ******** VCF
MF21, ..., MF2n ... ******** VCF
MUL181, ..., MUL18n ... Multiplication circuit
OP21, OP22, OP25, OP26, OP27 ... Operation amplifying circuit
P1, P2, and P3 ... peak
R (t) ... Input signal
RS11, ..., RS1n ... re-diffusion circuit
SH191, ..., SH19n ... sample hold circuit
Vth ... Threshold voltage.
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[Translation done.]

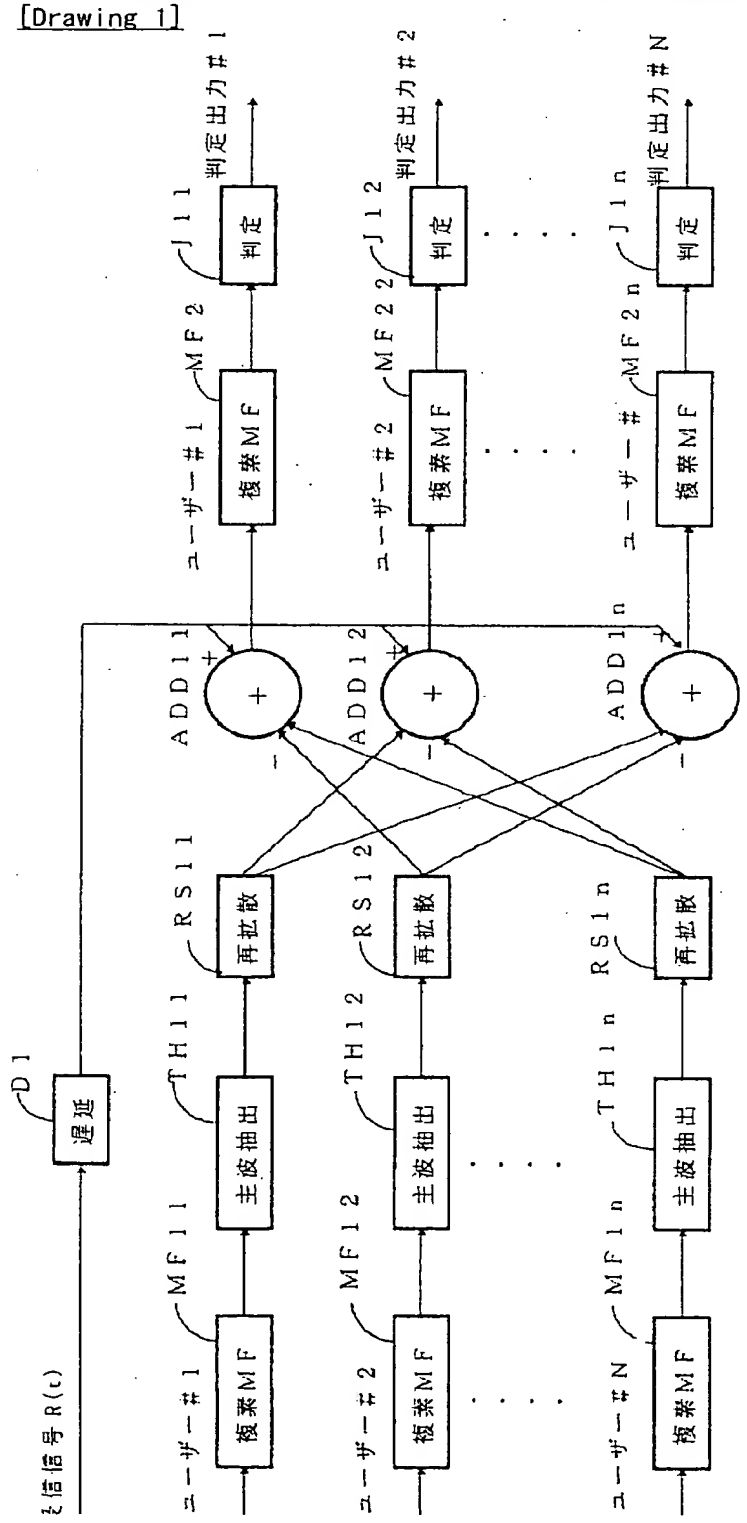
* NOTICES *

The Japanese Patent Office is not responsible for any damages caused by the use of this translation.

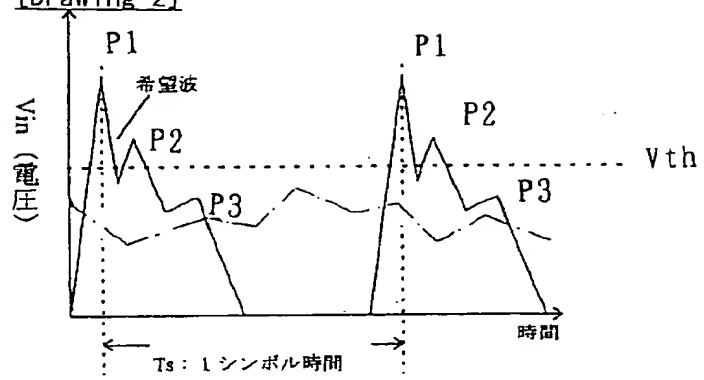
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

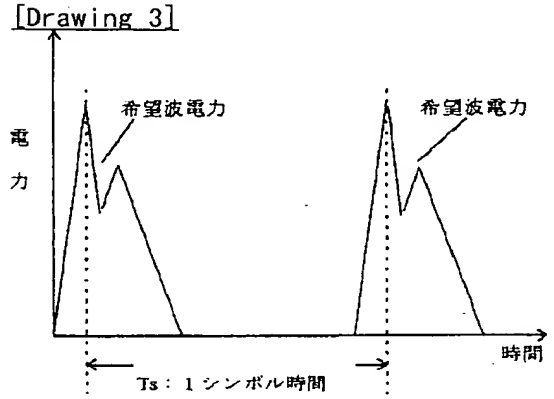
[Drawing 1]



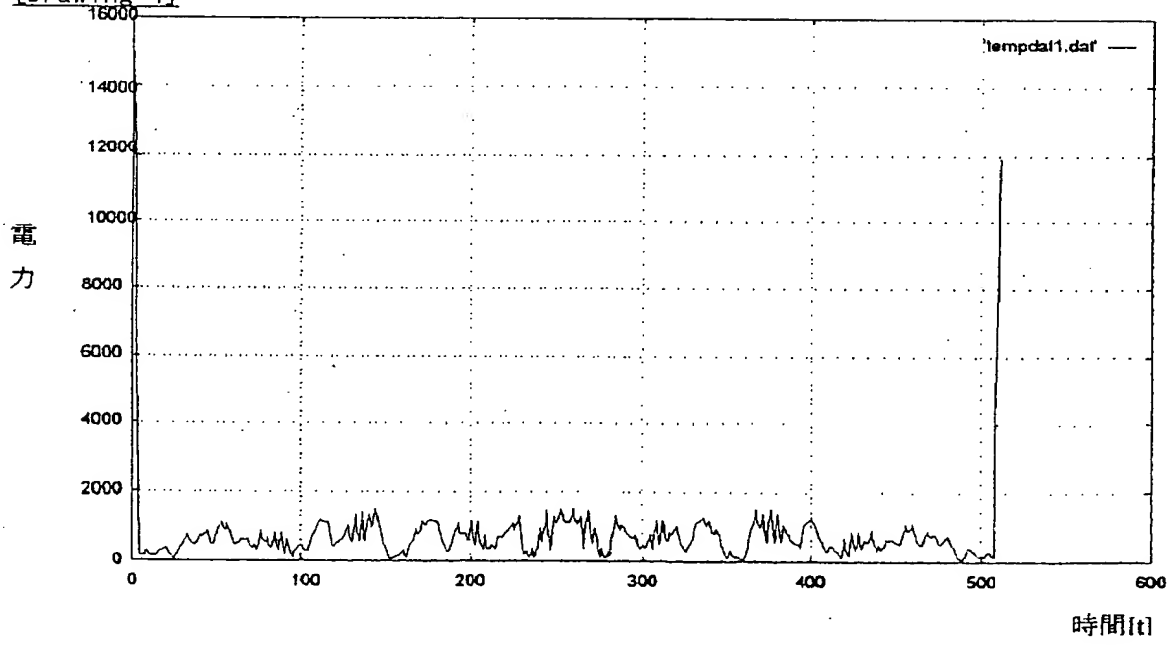
[Drawing 2]



[Drawing 3]



[Drawing 4]



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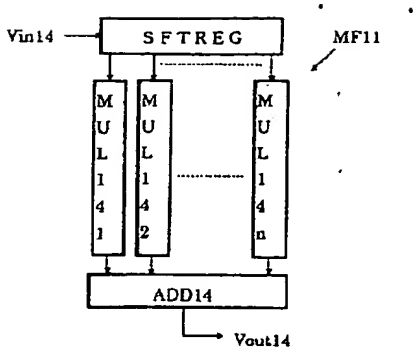

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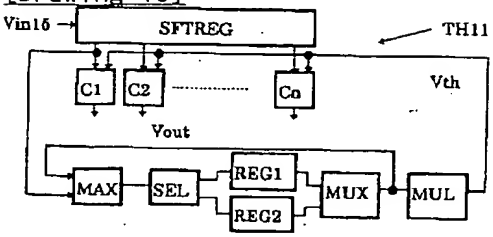

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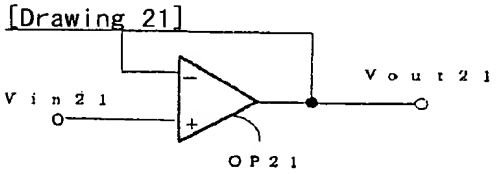

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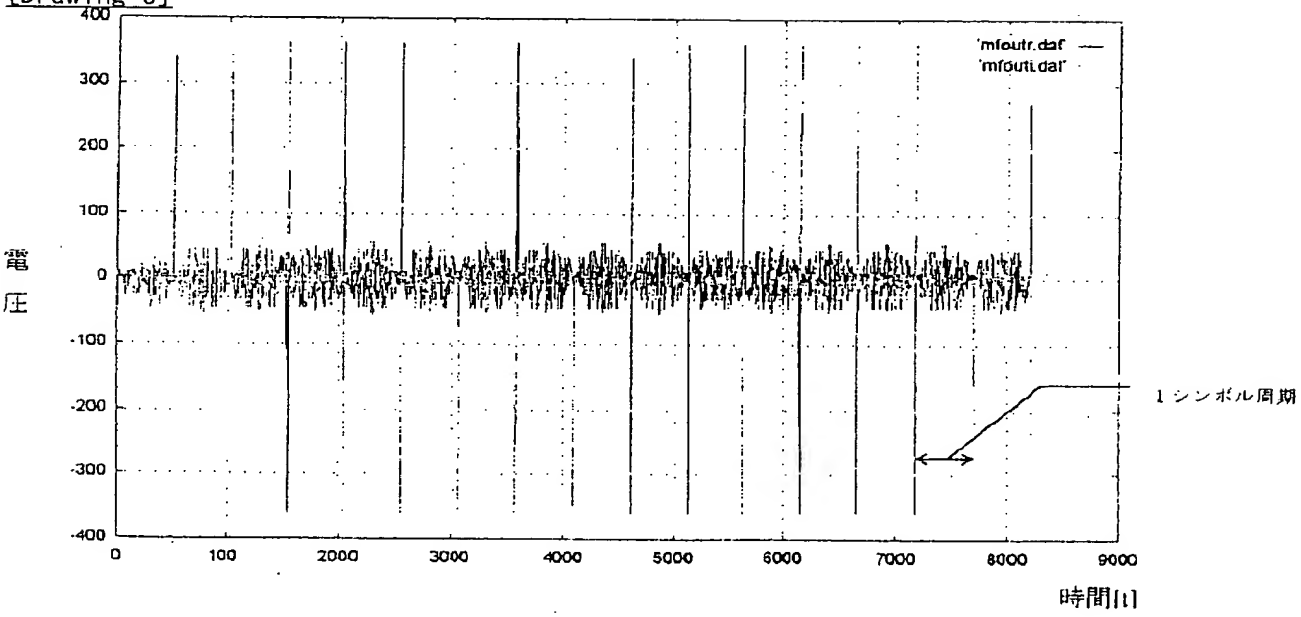

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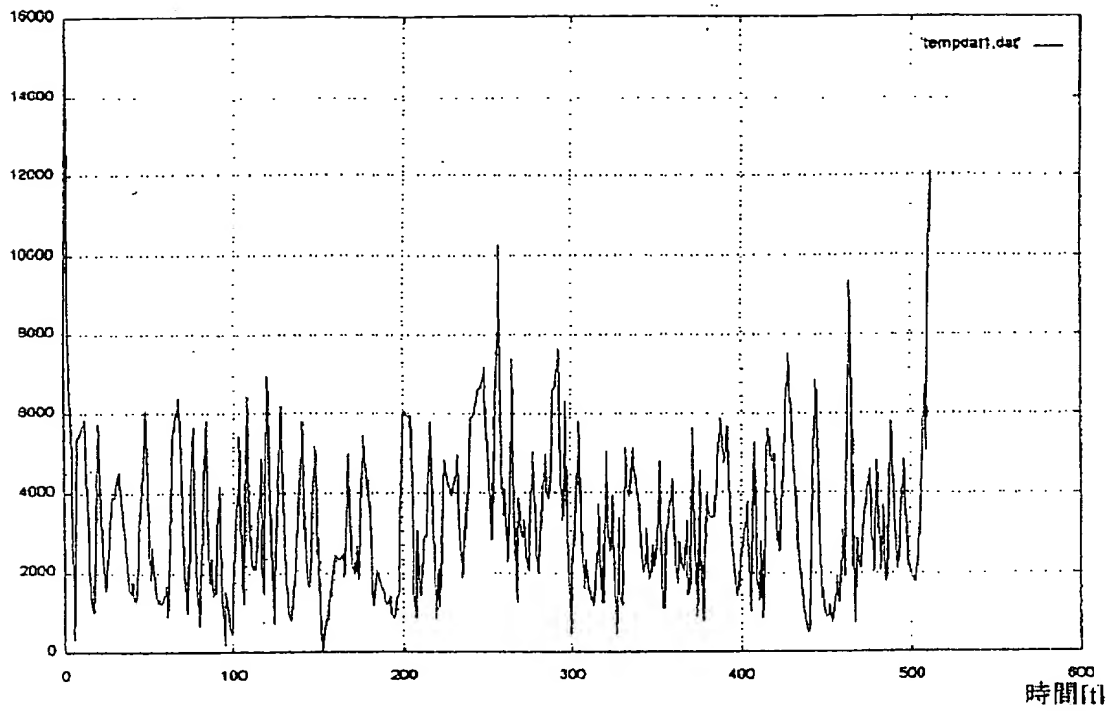

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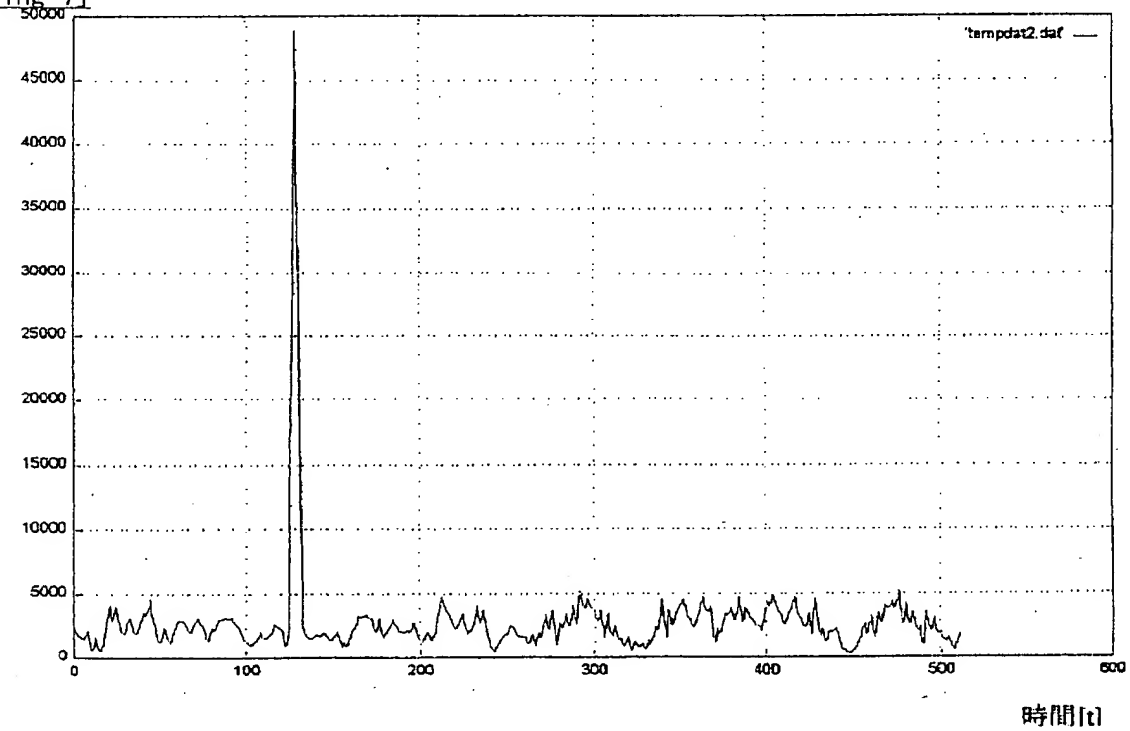

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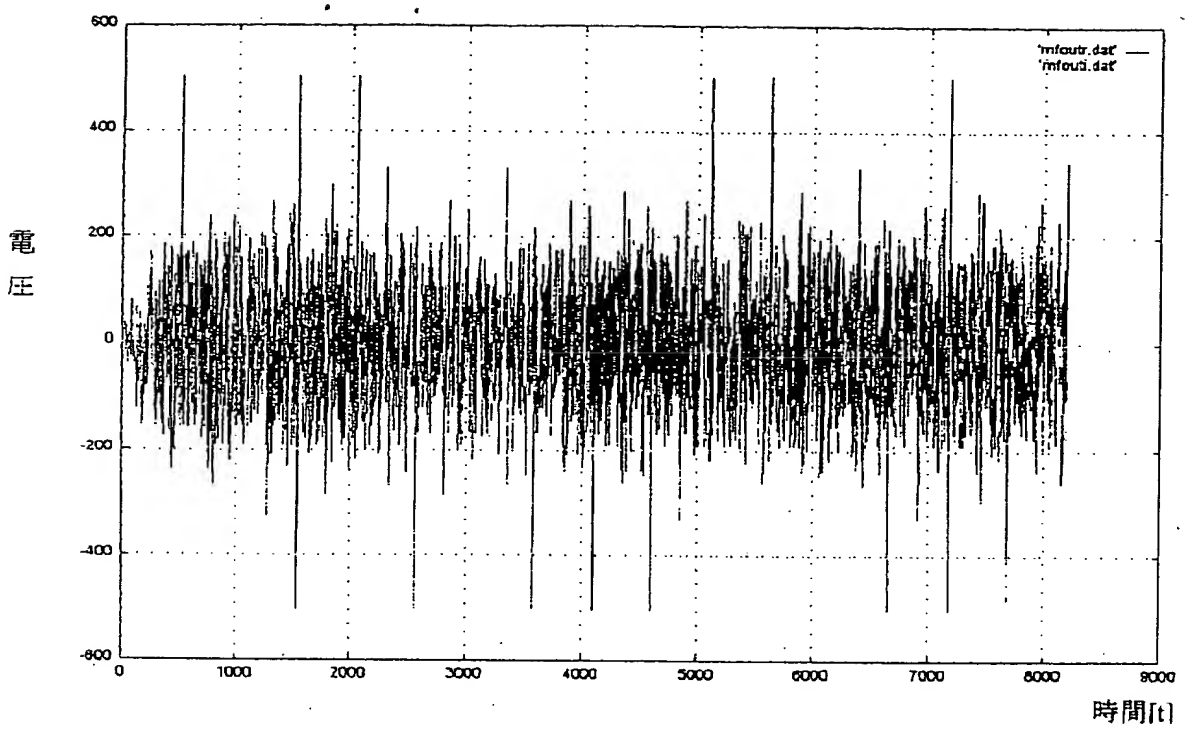

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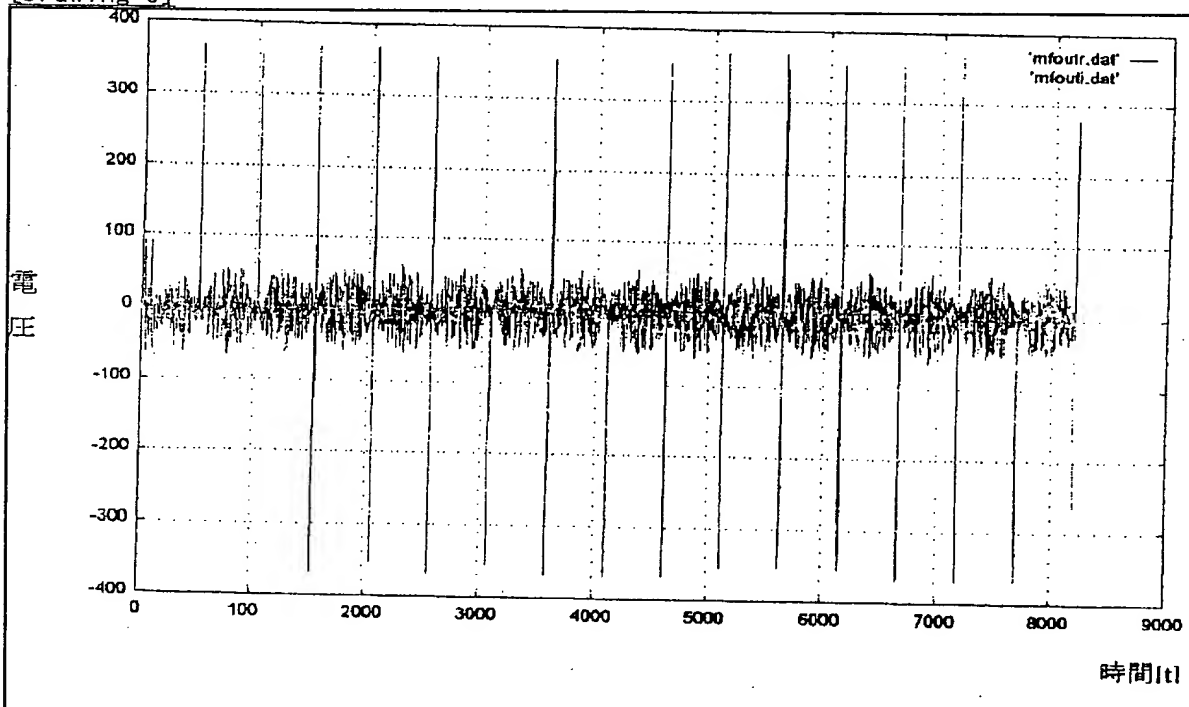

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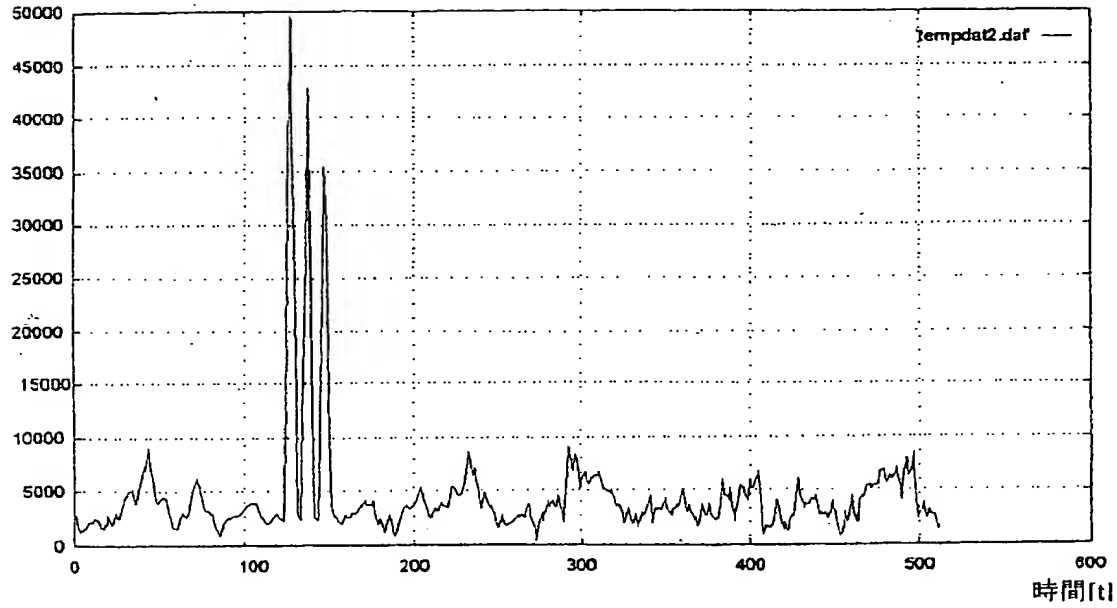

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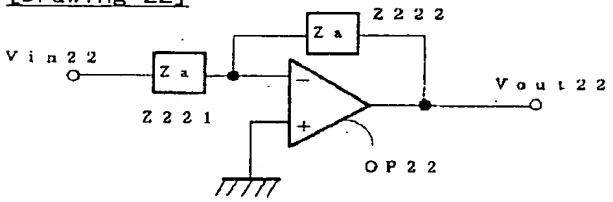

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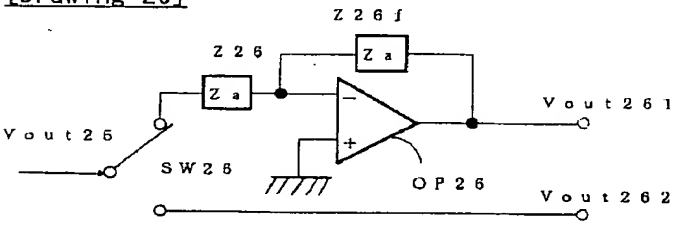

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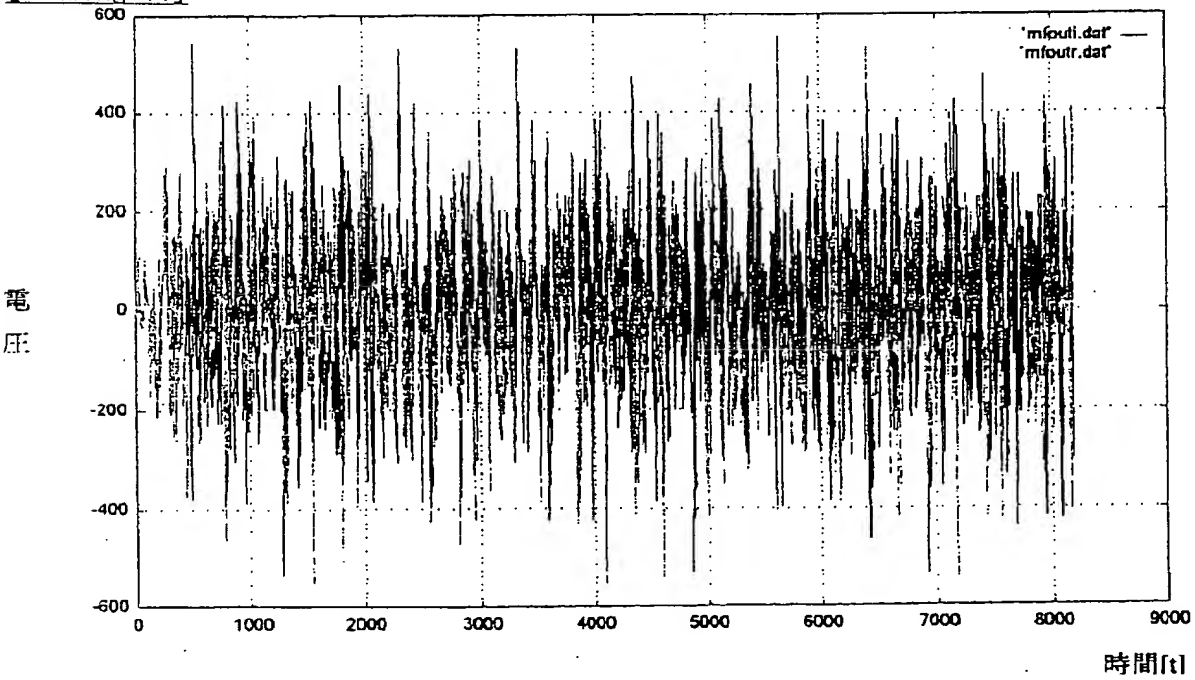

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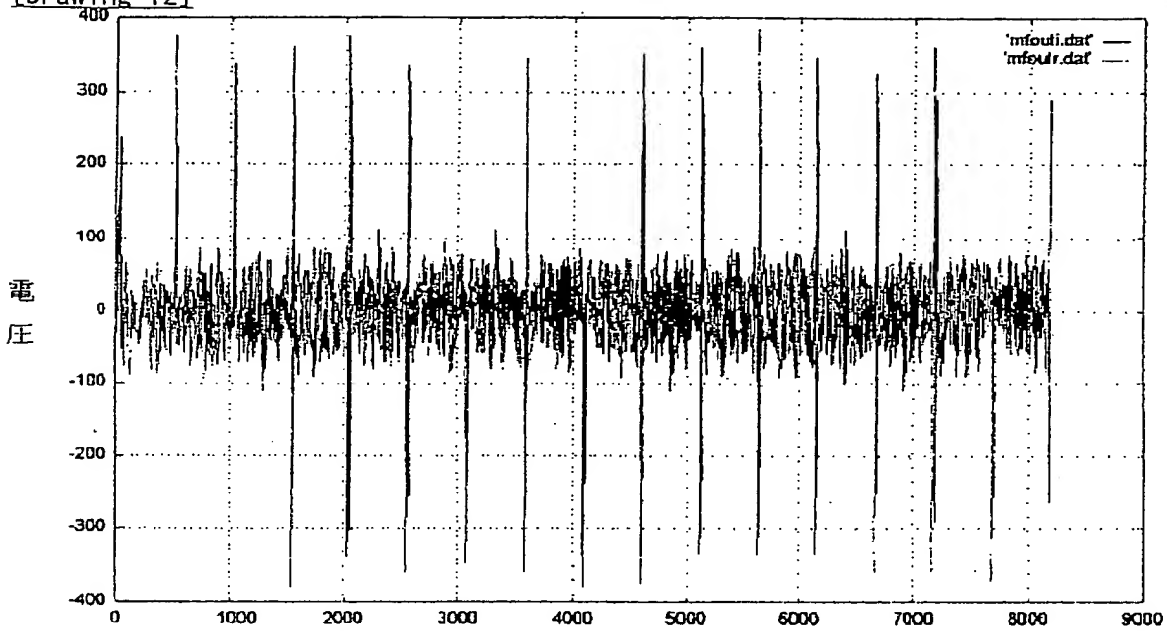

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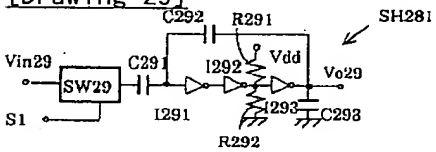

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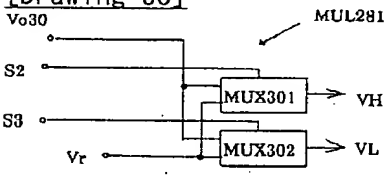

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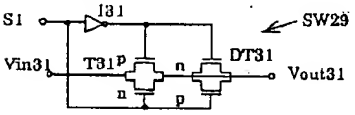
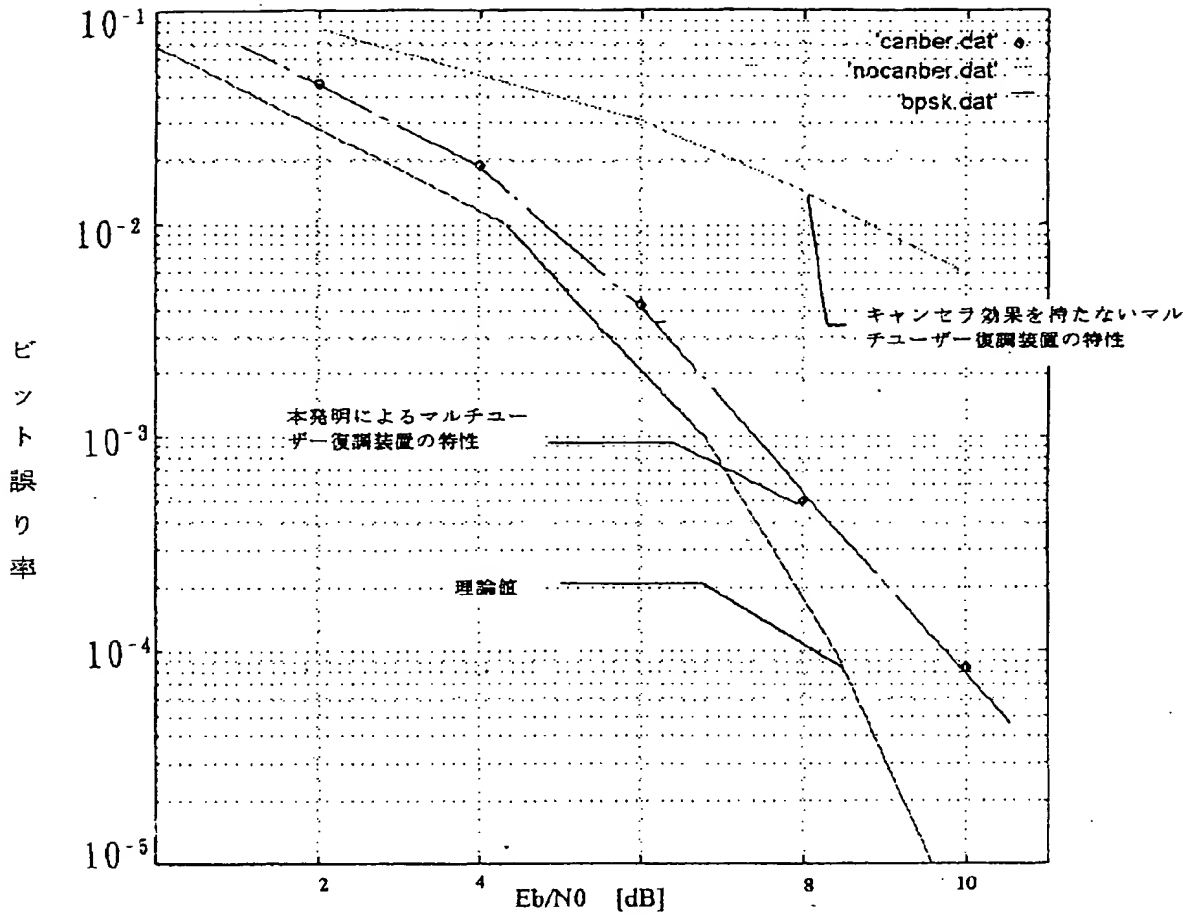


[Drawing 13]



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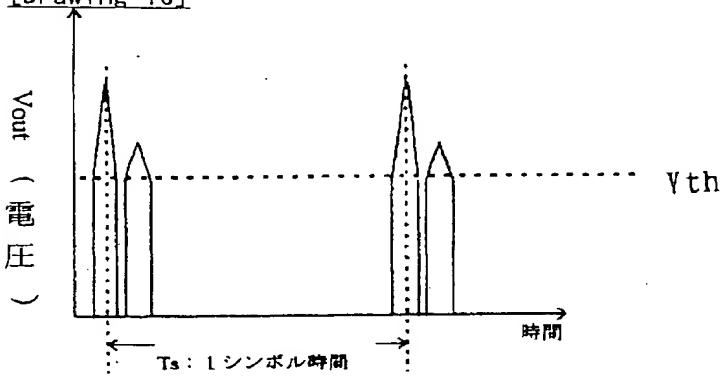

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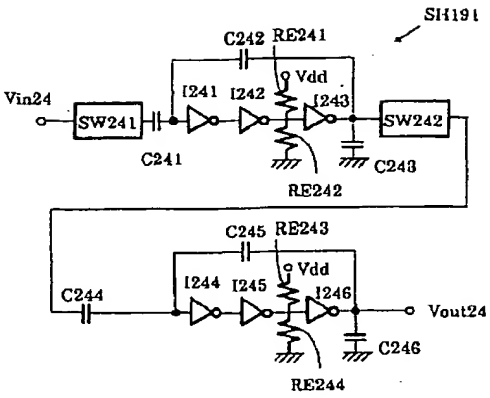

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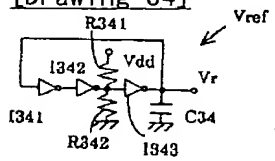

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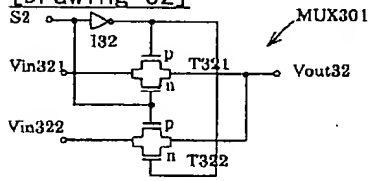

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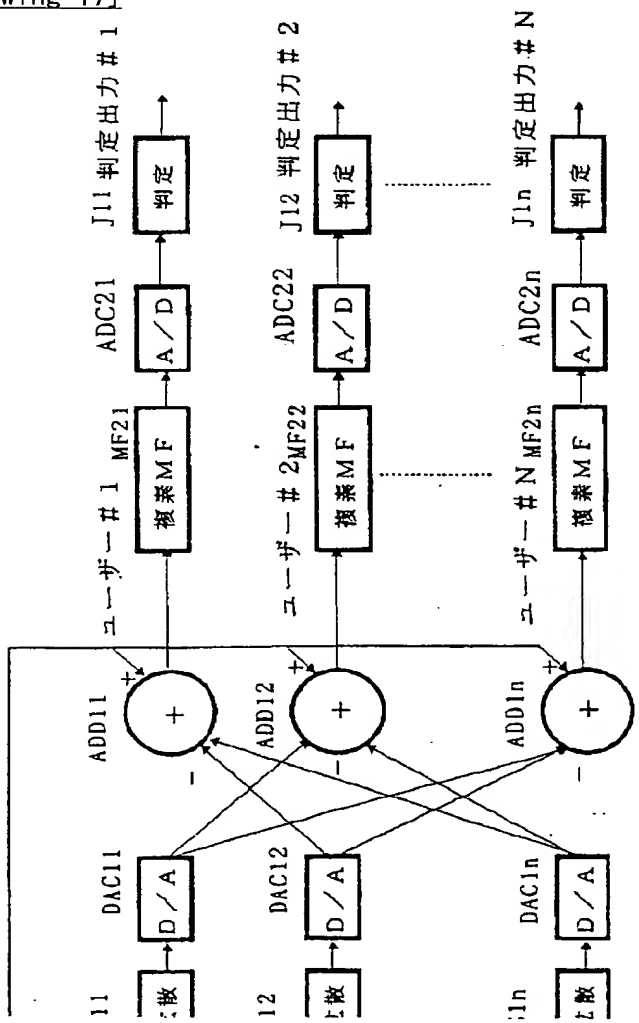

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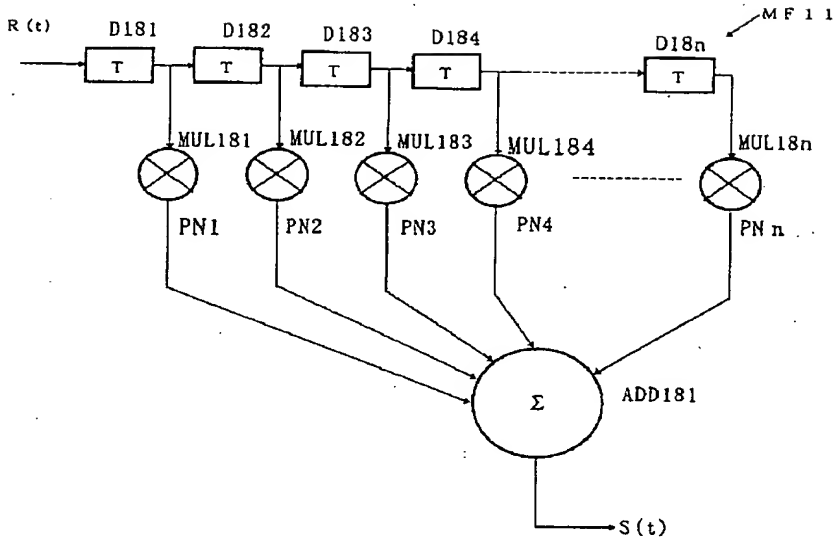

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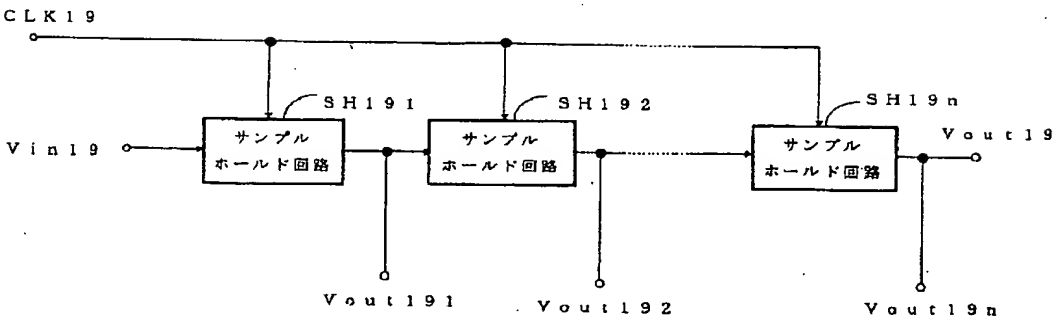

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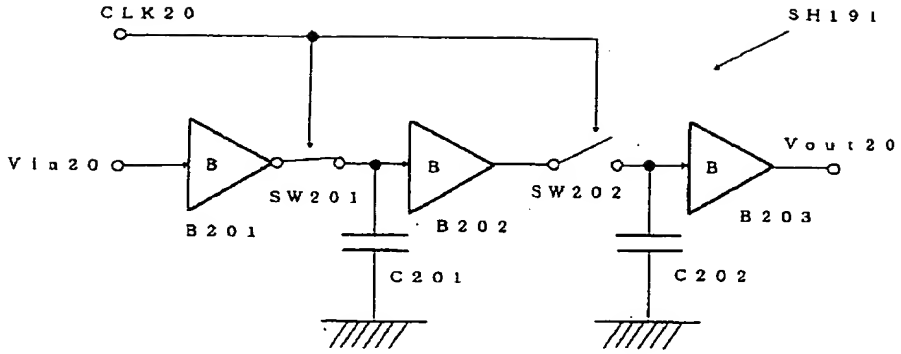

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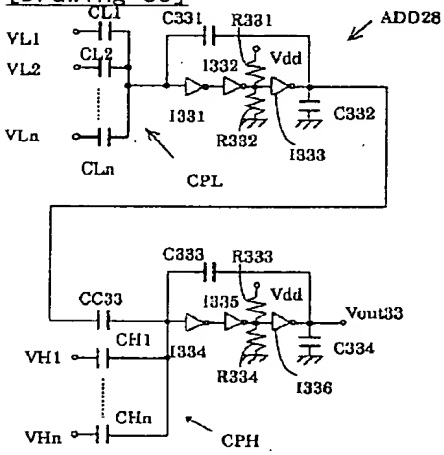

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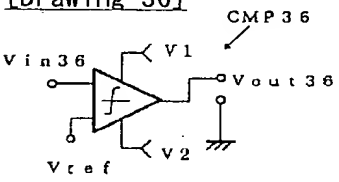

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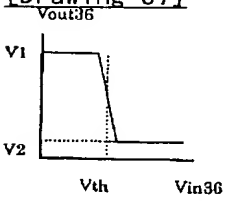

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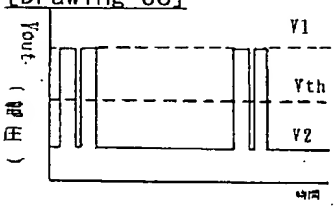

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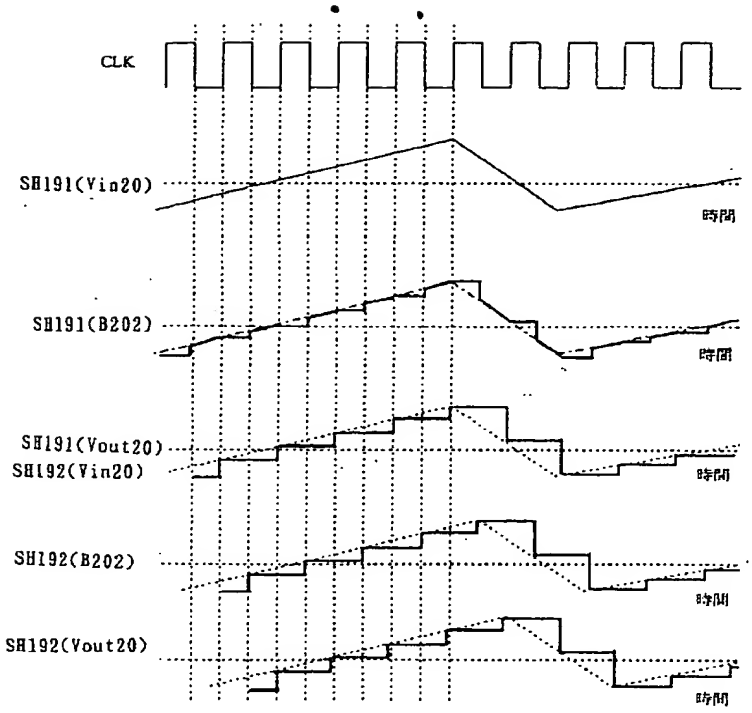

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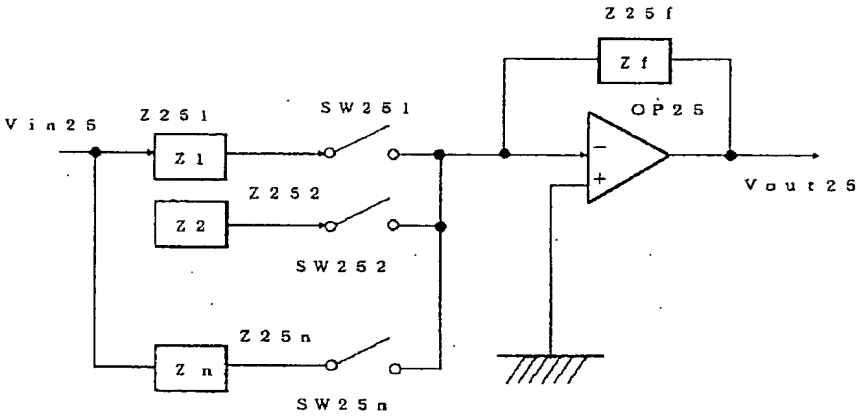

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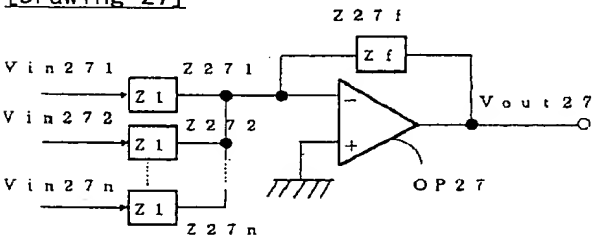
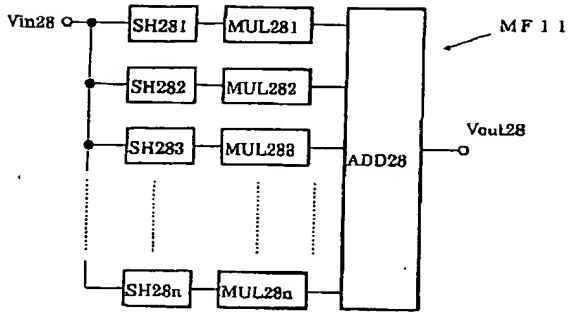
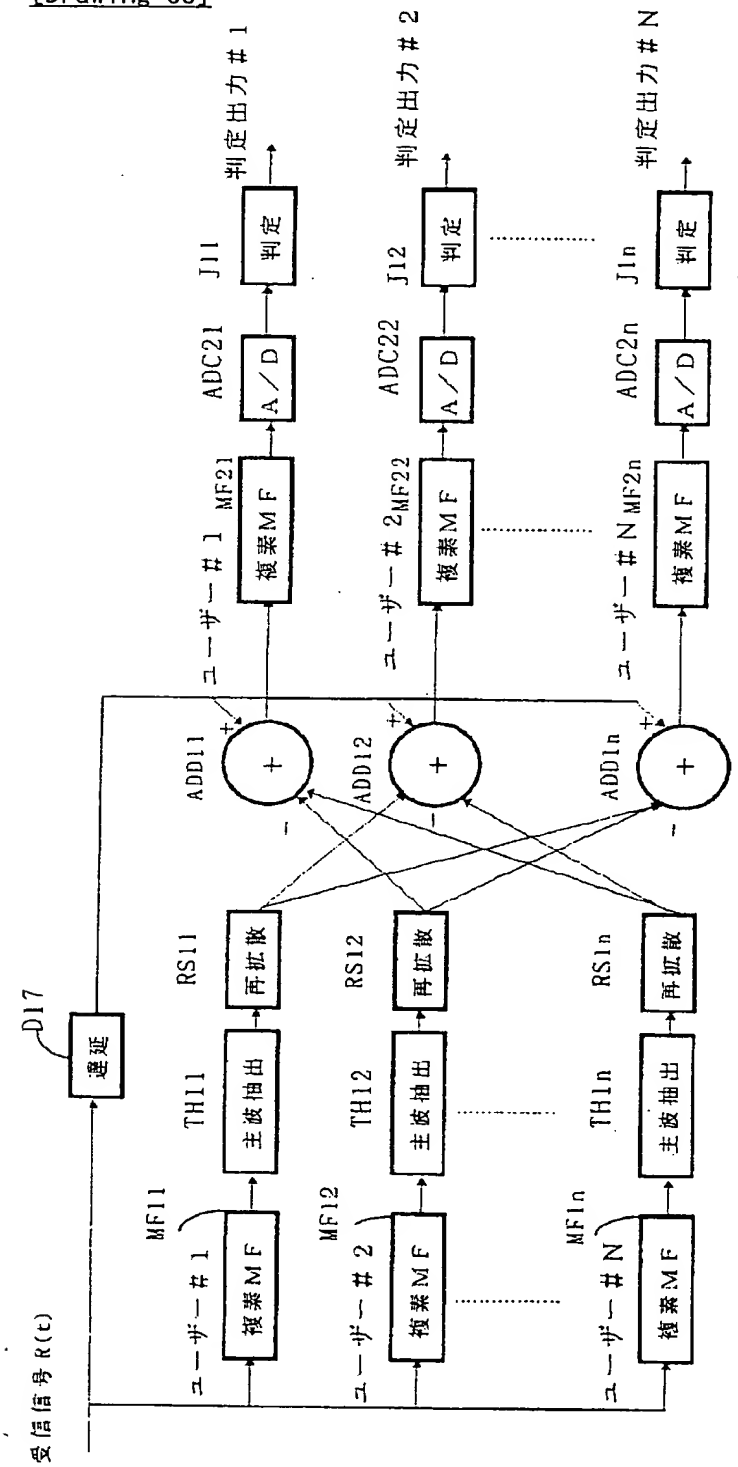


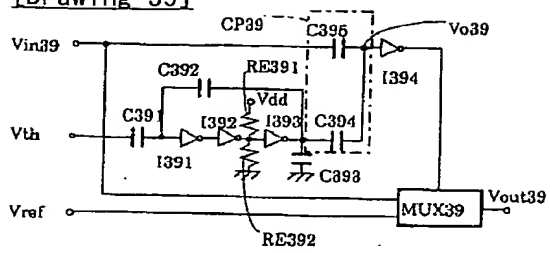
[Drawing 28]


Vin28
SH281
MUL281
SH282
MUL282
SH283
MUL283
SH28n
MUL28n
ADD28
MF11
Vout28

[Drawing 35]


受信信号R(t)
D17
遅延
ユーザー#1
ユーザー#2
ユーザー#N
MF11
MF12
MF1n
複素MF
TH11
TH12
TH1n
主波抽出
RS11
RS12
RS1n
再拡散
ADD11
ADD12
ADD1n
ユーザー#1 MF21
ユーザー#2 MF22
ユーザー#N MF2n
ADC21
ADC22
ADC2n
A/D
J11
J12
J1n
判定
判定出力#1
判定出力#2
判定出力#N

[Drawing 39]



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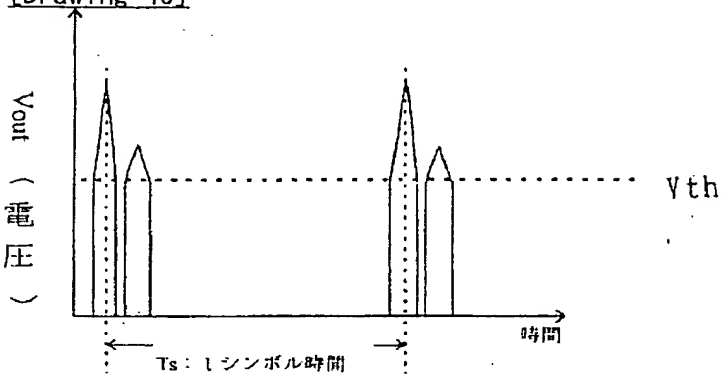

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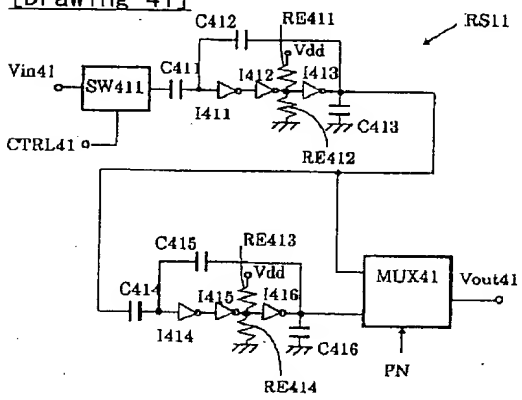

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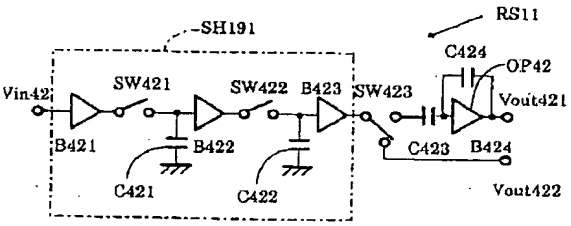

[Translation done.]